CIO-DIO48

USER'S MANUAL

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1 INTRODUCTION

This manual provides complete information on all of Computer Boards' digital I/O boards and accessories which follow the 50 pin connector form factor. The manual is organized into separate sections for those aspects of a product which are unique. Some issues, such as BASIC programming and electronic interfacing are applicable to all of the digital boards.

There are three digital I/O boards which use the 50 pin header type connector. These are the CIO-DIO48, CIO-DIO96 and CIO-DIO192.

The CIO-DIO48 has two 82C55 parallel interface chips and a 50 pin connector. Each 82C55 controls 24 CMOS TTL digital I/O pins. Within each 82C55, the digital I/O lines may be programmed as groups of 8,8 & 8 or 8,8 & 4,4). Each group may be input or output.

The CIO-DIO96 is exactly two CIO-DIO48 circuits on a single board.

The CIO-DIO192 is exactly 4 CIO-DIO48 circuits on a single board.

The CIO-DIO48H is a high drive, 48 line digital I/O board built up of logic chips. The control registers which set the direction of the I/O ports are identical to 82C55 mode 0 control registers (like those on the CIO-DIO48 in mode 0). The I/O lines are high drive, capable of sourcing 15mA and sinking 60mA.

All these boards have the same connector pin-out and respond to the same software instructions. Each board is explained in detail.

There is information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2 must procure a data book from Intel Corporation Literature Department. Call 800-548-4725 and order Part No. 230843 Micro and Peripherals Handbook, a 2 volume set. As of this writing, the data books are free of charge.

A BASIC CALL is provided with the board. The section on BASIC CALL programming is applicable to all of the CIO digital boards. Every board is supported by the BASIC CALL. Details will be found in the section on BASIC programming.

A group of application notes discusses electrical interfacing. If you have an interesting application note, please forward it to us for inclusion.

The goal of this manual is to assist you in your application of a CIO board to your sensing or control problem. We are interested in your corrections and suggestions and will implement them.

As an owner of a Computer Boards product, you are entitled to the latest revision of the manual and software. Just call with your current revision numbers handy, and request an update be sent to you.

2 SOFTWARE INSTALLATION

InstaCal is an installation, calibration and test package. Use it to guide the installation procedure and to calibrate your data acquisition board. InstaCal also creates a configuration file required for programmers who have purchased the Universal Library programming libraries.

Use the test option to verify the installation.

IOTEST may also be used to verify the installation. It exercises the CIO-DAS1600 by stimulating the analog and digital output ports and reading the analog and digital inputs. The inputs are displayed on the screen on a line graph.

IOTEST can provide one output and read one input at a time. The activity on an output channel is fixed by the program. Analog output 0 and 1 produce a sine wave. Digital outputs produce a square wave. Counter outputs produce a square wave.

3 QUICK START

The CIO-DIO48[1] is easy to use. Here is the quick start procedure for those who know how to open the PC and install expansion boards, and want to dive right in.

BOARD SETUP: The CIO-DIO48 is setup at the factory with:

BASE ADDRESS	300H (768 Decimal) Same as data sheet.
WAIT STATE	CIO-DIO48, WAIT STATE, Off position, Right.
	CIO-DIO48H, WS1, Off position, Right

Open your PC (after turning off the power) and install the board. Leave the switches as they were set at the factory or refer to the data sheet to change the settings. They are described in detail on the data sheet and in this manual. After the board is installed and the computer is closed up, turn the power back on.

SOFTWARE SETUP: Use IOTEST.EXE from the CIO-DIO Utility Disk, or,

Answer your software program setup questions with the information above. The *Compatible I/O Series*[TM] utility software and drivers are preconfigured.

SIGNAL CONNECTION

The CIO-DIO is a digital input and output device. Digital inputs require 2 connections be made from the signal source to the CIO-DIO. These are SIGNAL & GROUND. Signals should be TTL compatible: 0 to 0.8V low, 2.4V to 5V high

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1 The part number CIO-DIO48 is used throughout the manual because each of the products treated in this manual is comprized of CIO-DIO48 blocks on a single board.
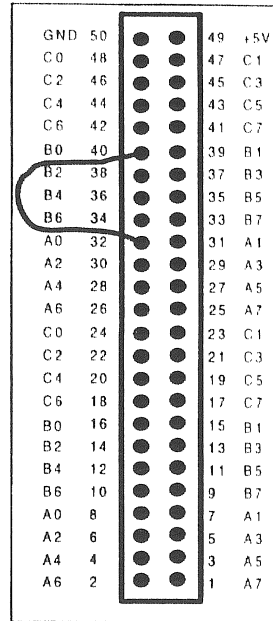
To test the digital inputs you need a known signal to connect to them. The simplest signal to connect is a digital output to a digital input. The program IOTEST produces a square wave on a digital output, reads it on a digital input, and displays the square wave on the screen.

Using the shorting wires supplied with the board, short pins together as shown to the right.

Run the program 'IOTEST' on the CIO-DIO utility disk. Select digital output as bit #1 and digital input as bit #9. You should see a slow moving square wave on the screen.

If you see the square wave, the CIO-DIO is installed and running correctly. You may now run other programs from the utility disk or install and run LABLOG2.

NOTE: IOTEST requires a CGA, EGA or VGA video display driver board to see a moving signal.

GND	50	● ●	49	+5V
C0	48	● ●	47	C1
C2	46	● ●	45	C3
C4	44	● ●	43	C5
C6	42	● ●	41	C7
B0	40	● ●	39	B1
B2	38	● ●	37	B3
B4	36	● ●	35	B5
B6	34	● ●	33	B7
A0	32	● ●	31	A1
A2	30	● ●	29	A3
A4	28	● ●	27	A5
A6	26	● ●	25	A7
C0	24	● ●	23	C1
C2	22	● ●	21	C3
C4	20	● ●	19	C5
C6	18	● ●	17	C7
B0	16	● ●	15	B1
B2	14	● ●	13	B3
B4	12	● ●	11	B5
B6	10	● ●	9	B7
A0	8	● ●	7	A1
A2	6	● ●	5	A3
A4	4	● ●	3	A5
A6	2	● ●	1	A7

4 OPERATION

4.1 INSTALATION

The CIO-DIO48 has two 82C55 parallel interface chips and a 50 pin connector. Each 82C55 controls 24 CMOS TTL digital I/O pins. Within each 82C55, the digital I/O lines may be programmed as groups of 8,8 & 8 or 8,8 & 4,4). Each group may be input or output.

The CIO-DIO96 is eaxactly two CIO-DIO48 circuits on a single board.

The CIO-DIO192 is exactly 4 CIO-DIO48 circuits on a single board.

All three boards share in common a base address switch, wait state jumper and 50 pin   ector(s)

4.1.1 BASE ADDRESS

The IOTEST program will request that you 'SELECT BASE ADDRESS', which allows you to choose a desired base address and adjusts the base address if necessary to place it on an 8 bit boundary, CIO-DIO48, 16 bit boundary, CIO-DIO96 or 32 bit boundary, CIO-DIO192

The CIO-DIO employs the PC bus for power, communications and data transfer. As such it draws power from the PC, monitors the address lines and control signals and responds to it's I/O address, and it receives and places data on the 8 data lines.

The BASE address is the most important user selectable bus related feature of the CIO-DIO. The base address is the location that software writes to and reads from when communicating with the CIO-DIO.

The base address switch is the means for setting the base address. Each switch position corresponds to one of the PC bus address lines. By placing the switch down, the CIO-DIO address decode logic is instructed to respond to that address bit.

A complete address is constructed by calculating the HEX or decimal number which corresponds to all the address bits the CIO-DIO has been instructed to respond to. For example, shown to the right are address 9 and 8 UP, all others DOWN.

Address 9 = 200H (512D) and address 8 = 100H (256D), when added together they equal 300H (768D).

NOTE: DO NOT PAY ATTENTION TO THE NUMBERS PRINTED ON THE SWITCH. LOOK AT THE NUMBERS PRINTED IN WHITE ON THE BOARD!

Address 300H shown	SW	HEX
	A9	200
	A8	100
	A7	80
	A6	40
	A5	20
	A4	10
	A3	8
9 8 7 6 5 4 3 2	A2	4

↓ ↓ ↑ ↑ ↑ ↑ ↑ ↑

Certain address are used by the PC, others are free and may be used by the CIO-DIO and other expansion boards. We recommend BASE = 300H (768D) be tried first.

TABLE OF I/O ADDRESS

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	82C55 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)		300-30F PROTOTYPE
CARD			
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

The CIO-DIO BASE switch may be set for address in the range of 000-3F0 so it should not be hard to find a free address area for you CIO-DIO. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31F HEX are free to use.

Addresses not specifically listed, such as 390-39F, are free.

4.1.2 WAIT STATE JUMPER

The CIO-DIO boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DIO board so that signals from slow devices (chips) will be valid.

The wait state generator on the CIO-DIO is only active when the CIO-DIO is being accessed. Your PC will not be slowed down in general by using the wait state.

Because all PC expansion board busses are slowed to either 8MHz or 10MHz, the wait state will generally not be required.

If you experience sporadic errors from the 82C55 digital I/O chip (reset, port direction swaps) you might try enabling the wait state generator.

Wait State Jumper Block

O O
N F
F
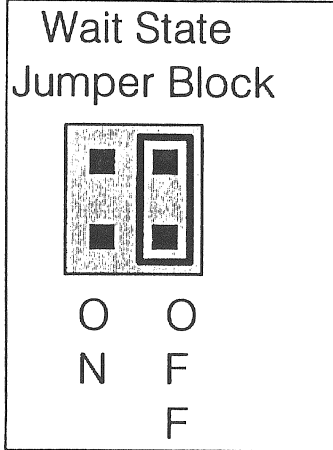
4.1.3 INSTALLING THE CIO-DIO IN THE COMPUTER

Turn the power off.

Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DIO.

4.1.4 CABLING TO THE DIO CONNECTOR

The CIO-DIO48 connector is accessible through the PC/AT expansion bracket. The connector is a standard 50 pin male header connector. A mating female connector my be purchased from Computer Boards, at Radio Shack or other electronic supply outlets.

4.2 SIGNAL CONNECTION - CIO-DIO48

All the digital outputs inputs on the CIO-DIO48 connector are CMOS TTL. TTL is an electronics industry term, short for Transistor Transistor Logic, which describes a standard for digital signals which are either at 0V or 5V. The binary logic inside the PC is all TTL or LSTTL (Low power Schotky TTL).

Under normal operating conditions, the voltages on the 82C55 pins range from 0 to 0.45 volts for the low state to between 2.4 to 5.0 volts for the high state. At a voltage of 0.45 volts the 82C55 can safely sink 2 mA. At a voltage of 2.4 volts the 82C55 can source 0.4 mA. These values are typical of TTL devices.

The voltages and currents associated with external devices range from less than a hundred mA at a few volts for a small flash light bulb to 50 Amps at 220 volts for a large electric range. Attempting to connect either of these devices directly to the CIO-DIO would destroy the I/O chip.

In addition to voltage and load matching, digital signal sources often need to be de-bounced. A complete discussion of digital interfacing will be found in the section on Interface Electronics in this manual.

IMPORTANT NOTE: The 82C55 digital I/O chip initializes all ports as inputs on power up and reset. A TTL input is a high impedence input. If you connect another TTL input device to the 82C55 it will probably be turned ON every time the 82C55 is reset, or, it might be turned OFF instead. Remember, and 82C55 which is reset is in INPUT mode.

To safegaurd against unwanted signal levels, all devices being controlled by an 82C55 should be tied low (or high, as required) by a 10K ohm resistor.

You will find positions for pull up and pull down resistor packs on your CIO-DIO board. To impliment these, please turn to the application note on pull up/down resistors.

UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float. If you are using a DIO board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0... It is unconnected and so is not specified. The 82C55 is not malfunctioning. In the absence of a pull-up/down resistor, any input to a CIO-DIO which is unconnected is unspecified.
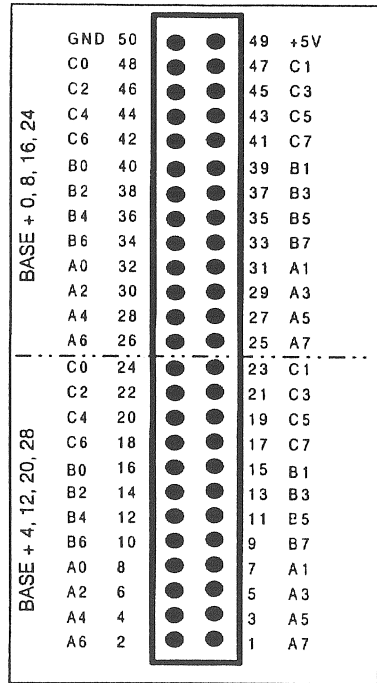
You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software.

4.3 CONNECTOR DIAGRAM

The CIO-DIO48 I/O connector is a 50 pin D type connector accessible from the rear of the PC through the expansion backplate. The signals available are direct connections to an 82C55 digital I/O chip.

The connector accepts female 50 pin header connectors, such as those on the C50FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERM100, CIO-SPADE50 and CIO-MINI50 screw terminal boards.

BASE + 0, 8, 16, 24			
GND	50	49	+5V
C0	48	47	C1
C2	46	45	C3
C4	44	43	C5
C6	42	41	C7
B0	40	39	B1
B2	38	37	B3
B4	36	35	B5
B6	34	33	B7
A0	32	31	A1
A2	30	29	A3
A4	28	27	A5
A6	26	25	A7

BASE + 4, 12, 20, 28			
C0	24	23	C1
C2	22	21	C3
C4	20	19	C5
C6	18	17	C7
B0	16	15	B1
B2	14	13	B3
B4	12	11	B5
B6	10	9	B7
A0	8	7	A1
A2	6	5	A3
A4	4	3	A5
A6	2	1	A7

4.4 ARCHITECTURE

4.4.1 82C55 CONTROL & DATA REGISTERS

Each CIO-DIO is composed of 82C55 parallel I/O chips. Each chip contains 3 data and one control register occupying 4 consecutive I/O locations. The number of I/O locations occupied by a CIO-DIO board is equal to 4 times the number of 82C55 chips on the board.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to. Most often, register manipulation is best left to ASSEMBLY language programs as most of the CIO-DIO possible functions are implemented in an easy to use BASIC CALL.

The register descriptions follow all follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE + 0	Port A Input of 82C55	Port A Output
BASE + 1	Port B Input	Port B Output
BASE + 2	Port C Input	Port C Output
BASE + 3	None. No read back on 82C55.	Configure 82C55
BASE + 4	Port A Input of 82C55	Port A Output
BASE + 5	Port B Input	Port B Output
BASE + 6	Port C Input	Port C Output
BASE + 7	None. No read back on 82C55.	Configure 82C55
	ADDITIONAL CIO-DIO96 & 192 ONLY	
BASE + 8	Port A Input of 82C55	Port A Output
BASE + 9	Port B Input	Port B Output
BASE + 10	Port C Input	Port C Output
BASE + 11	None. No read back on 82C55.	Configure 82C55
BASE + 12	Port A Input of 82C55	Port A Output
BASE + 13	Port B Input	Port B Output
BASE + 14	Port C Input	Port C Output
BASE + 15	None. No read back on 82C55.	Configure 82C55
	ADDITIONAL CIO-DIO192 ONLY	
BASE + 16	Port A Input of 82C55	Port A Output
BASE + 17	Port B Input	Port B Output
BASE + 18	Port C Input	Port C Output
BASE + 19	None. No read back on 82C55.	Configure 82C55
BASE + 20	Port A Input of 82C55	Port A Output
BASE + 21	Port B Input	Port B Output
BASE + 22	Port C Input	Port C Output
BASE + 23	None. No read back on 82C55.	Configure 82C55
BASE + 24	Port A Input of 82C55	Port A Output
BASE + 25	Port B Input	Port B Output
BASE + 26	Port C Input	Port C Output
BASE + 27	None. No read back on 82C55.	Configure 82C55

BASE + 28	Port A Input of 82C55	Port A Output
BASE + 29	Port B Input	Port B Output
BASE + 30	Port C Input	Port C Output
BASE + 31	None. No read back on 82C55.	Configure 82C55

4.4.1.1 82C55 DIGITAL I/O REGISTERS

PORT A DATA
BASE ADDRESS + 0   300 HEX, 768 Decimal

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
Pin 30	Pin 31	Pin 32	Pin 33	Pin 34	Pin 35	Pin 36	Pin 37

PORT B DATA
BASE ADDRESS + 1   301 HEX, 769 Decimal

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10

Ports A & B may be programmed as input or output. Each is written to and read from in Bytes, although for control and monitoring purposes the individual bits are more interesting.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS + 2   302 HEX, 770 Decimal

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1
128 Bit	64 Weight	32 Dec.	16	8	4	2	1
80 Bit	40 Weight	20 HEX	10	8	4	2	1
Pin 21	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28	Pin 29

Port C may be used as one 8 bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output. The notation for the upper 4 bit port is PCH3 - PCH0, and for the lower, PCL3 - PCL0.

Although it may be split, every read and write to port C carries 8 bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS

In 82C55 mode 0 configuration, ports configured for output hold the output data written to them. This output byte may be read back by reading a port configured for output.

INPUT PORTS

In 82C55 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel or AMD data book and see the 82C55 data sheet.

82C55 CONTROL REGISTER
BASE ADDRESS + 3   303 HEX, 771 Decimal

7	6	5	4	3	2	1	0
MS	M3	M2	A	CU	M1	B	CL
	Group A				Group B		

The 82C55 may be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

Included here is information on programming the 82C55 in mode 0. Those wishing to use the 82C55 in modes 1 or 2, must procure a data book from Intel Corporation Literature Department. Call 800-548-4725 and order Part No. 230843 Micro and Peripherals Handbook, a 2 volume set. As of this writing, the data books are free of charge.

When the PC is powered up or RESET, the 82C55 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 82C55 for other modes, the following control code byte must be assembled into on 8 bit byte.

MS = Mode Set. 1 = mode set active

M3	M2	Group A Function	
0	0	Mode 0	Input / Output
0	1	Mode 1	Strobed Input / Output
1	X	Mode 2	Bi-Directional Bus

A	B	CL	CH	Independent Function
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B.   Input / Output
M1 = 1 is mode 1 for group B.   Strobed Input / Output

The Ports A, B, C High and C Low may be independently programmed for input or output.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 82C55 in this mode are shown below. D7 is always 1 and D6, D5 & D2 are always 0.

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

4.5 SPECIFICATIONS

4.5.1 POWER CONSUMPTION

CIO-DIO48

+5V Supply	100 mA typical / 200 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO48H

+5V Supply	700 mA typical / 800 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO96

+5V Supply	190 mA typical / 320 mA max.
+12V Supply	None.
-12V Supply	None.

CIO-DIO192

+5V Supply	380 mA typical / 600 mA max.
+12V Supply	None.
-12V Supply	None.

NOTE   Additional power will be drawn by user's connections to the power pins accessible on CIO-DIO connectors.

4.5.2 DIGITAL I/O

TTL LEVEL DIRECT TO/FROM 82C55

82C55 output high	3.0 V min @ -2.5Ma
82C55 output low	0.4 V max @ 2.5 mA
82C55 input high	2.0 V min, 7 V max
82C55 input low	-0.5 V min, 0.8 V max
82C55 drive capability	5 LSTTL loads

HIGH DRIVE DIO48H

Output High	2.0V min @ -15mA
Output Low	0.55V max @ 64mA
Input High	2.0V min, 7.0V max
Input Low	0.8V max, -0.5V min

4.5.3 ENVIRONMENTAL

Operating Temperature	0 - 50 deg C
Storage Temperature	-20 to 70 deg C
Humidity	0 to 90% non-condensing
Weight	5 oz

5 ELECTRONICS AND INTERFACING

This short, simple introduction to the electronics most often needed by digital I/O board users covers a few key concepts. They are:

• Pull up/down resistors

- Transistors.
- Power MOSFETs
- Solid State Relays
- Voltage dividers.
- Low pass filters for digital inputs.
- Noise; sources and solutions.

IMPORTANT NOTE:

It cannot be stated often enough to those unfamiliar with the 82C55.

WHENEVER THE 82C55 IS POWERED ON OR RESET, ALL PINS ARE SET TO HIGH IMPEDENCE INPUT.

The implication of this fact is that if you have output devices such as solid state relays, they may be switched on whenever the computer is powered on or reset. To prevent unwanted switching and to drive all outputs to a known state after power on or reset, pull all pins either high or low through a 10K ohm resistor.

To install pull up/down resistor packs, see the application note.

5.1 PULL UP & PULL DOWN RESISTORS

This discussion deals with pul up/down resistors and 82C55 digital I/O chips on CIO-DIO boards.

Whenever the 82C55 is powered on or reset, the control register is set to a known state. That state is mode 0, all ports input.

When used as and output device to control other TTL input devices, the 82C55 applies a voltage level of 0V for low and 2.5V-5V for high. It is the output voltage level of the 82C55 that the device being controlled responds to.

The concept of voltage level of an 82C55 in input mode is meaningless. Do not connect a volt meter to the floating input of an 82C55. It will show you nothing of meaning. In input mode the 82C55 is in 'high Z' or high impedance. If your 82C55 was connected to another input chip (the device you were controlling), the inputs of that chip are left floating whenever the 82C55 is in input mode.

If the inputs of the device you are controlling are left to float, they may float up or down. Which way they float is dependent on the characteristics of the circuit and the electrical environment; and unpredictable! This is why it often appears that the 82C55 has gone 'high' after power up. The result is that you controlled device gets turned on!

That is why you need pull up/down resistors.

Shown here is one 82C55 digital output with a pull-up resistor attached.

The pull-up resistor provides a reference to +5V while its value of 10,000 ohms allows only 0.5mA of current to flow through the circuit.

If the 82C55 is reset and enters high impedance input, the line is pulled high. At that point, both the 82C55 AND the device being controlled will sense a high signal.

If the 82C55 is in output mode, the 82C55 has more than enough power to over ride the pull-up resistor's high signal and drive the line to 0 volts. If the 82C55 asserts a high signal, the pull up resistor guaranties that the line goes to +5V.
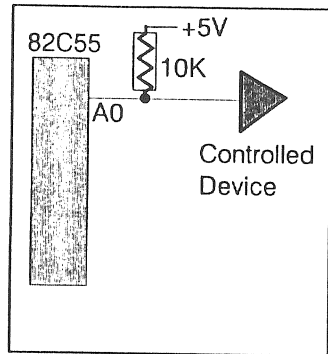
Of course, a pull-down resistor accomplishes the same task except that the line is pulled low when the 82C55 is reset. The 82C55 has more than enough power to drive the line high.

The CIO-DIO boards are equipped with positions for pull-up/down resistors Single Inline Packages (SIPs). The positions are marked A, B and C and are located beside the 82C55.

A 10K ohm, 8 resistor SIP is made of 8, 10K resistors all connected one side to a single common point and the other, each to a pin protruding from the SIP. The common line to which all resistor are connected also protrudes from the SIP. The common line is marked with a dot and is at one end of the SIP.

The SIP may be installed as pull-up or pull-down. At each location, A, B & C there are 10 holes in a line. One end of the line is +5V, the other end is GND. They are so marked. The 8 holes in the middle are connected to the 8 lines of the port, A, B, or C.

Install and solder the SIP in place.

A resistor value of 10K is recommended. Use other values only if you have calculated the necessity of doing so.

UNCONNECTED INPUTS FLOAT

Keep in mind that unconnected inputs float. If you are using a DIO board for input, and have unconnected inputs, ignore the data from those lines.

In other words, if you connect bit A0 and not bit A1, do not be surprised if A1 stays low, stays high or tracks A0... It is unconnected and so is not specified. The 82C55 is not malfunctioning. In the absence of a pull-up/down resistor, any input to a CIO-DIO which is unconnected is unspecified.

You do not have to tie input lines, and unconnected lines will not affect the performance of connected lines. Just make sure that you mask out any unconnected bits in software.

5.2 TTL TO SOLID STATE RELAYS

Many applications require digital outputs to switch AC and DC voltage motors on and off and to monitor AC and DC voltages. These AC and high DC voltages cannot be controlled or read directly by the TTL digital lines of a CIO-DIO.

Solid State Relays, such as those available from Computer Boards, Inc. allow control and monitoring of AC and high DC voltages and provide 750V isolation. Solid State Relays (SSRs) are the recommended method of interfacing to AC and high DC signals.

The most convenient way to use solid state relays and a CIO-DIO board is to purchase a Solid State Relay Rack. A SSR Rack is a circuit board with output buffer chips which are powerful enough to switch the SSR and sockets to plug SSRs into.

SSR Racks are available from Computer Boards and most manufacturers of SSRs.

If you only want to drive one or two SSRs, all you need is a 74LS244 output buffer chip between the 82C55 output and the SSR. Of course the SSR will need a 5 volt power source as well.

5.3 VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of a digital input, a voltage divider can drop the voltage of the input signal to the level the digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

Voltage = Current * Resistance

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.
The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the digital input and the maximum signal voltage.

SIMPLE VOLTAGE DIVIDER

$$\frac{Vin}{Vout} = \frac{R1 + R2}{R2}$$
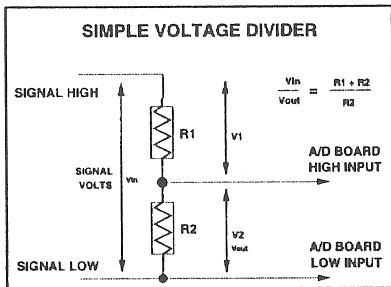
The phenomena of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

Attenuation =	$$\frac{R1 + R2}{R2}$$	The variable *Attenuation* is the proportional difference between the signal voltage max and the full scale of the analog input.
$2 =$	$$\frac{10K + 10K}{10K}$$	For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the *Attenuation* is 2:1 or just 2.
$R1 =$	$(A - 1) * R2$	For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs also make use of voltage dividers, for example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-DIO digital inputs. The voltage must be dropped to 5 volts max when on. The *Attenuation* is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

5.4 LOW PASS FILTERS DE-BOUNCE INPUTS

A low pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cut off frequency from entering the A/D board's analog *or* digital inputs.

The key term in a low pass filter circuit is **cut off frequency**. The cut of frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cut off frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25Hz would be allowed to pass.
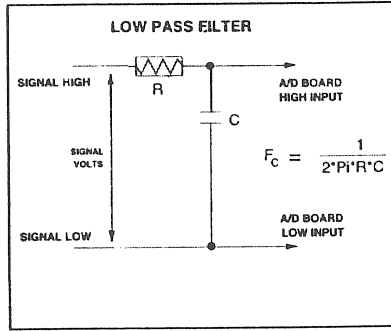
Also, in a digital circuit, a low pass filter might be used to de-bounce an input from a momentary contact button pushed by a person.

A low pass filter may be constructed from one resistor (R) and one capacitor (C). The cut off frequency is determined according to the formula:

$$F_c = \frac{1}{2 * Pi * R * C}$$

$$R = \frac{1}{2 * Pi * C * F_c}$$

Where Pi = 3.14...

LOW PASS FILTER

SIGNAL HIGH — R — A/D BOARD HIGH INPUT

SIGNAL VOLTS

$$F_c = \frac{1}{2*Pi*R*C}$$

SIGNAL LOW — A/D BOARD LOW INPUT

6 DIAGNOSIS & DEBUG

Computer Boards maintains technical support lines staffed by experienced Electrical Engineers and Technicians. There is no charge to call and calls are returned promptly if you have called when the lines were busy.

Most of the problems encountered with data acquisition plug in boards can be solved over the phone.

Signal connection and programming are the common sources of difficulty and Computer Boards' Tech Support people can solve these type of problems with you, especially if you prepare for the call.

1) Have the phone near the PC where you can try the things we suggest.

2) Be prepared to open the PC, remove the board and read back or change switch and jumper settings.

3) Have a volt meter available to make measurements of the signals you are trying to measure and the signals on the board and PC power supply.

4) Isolate the program lines that are not working as you expect them to.

5) Have all the source code to the program you are having trouble with so preceding modes and prerequisite modes may be discussed.

6) Have the manual ready.

7) Have the CIO-DIO Utility diskette available so the revision # and programs can be checked.

THIS LITTLE BIT OF PREPARATION WILL SPEED DIAGNOSIS AND MAY SAVE YOU THE TROUBLE OF A '.L BACK.

If you would like to try a few things first, here is a list of common problems.

1) Check the PC bus power.

2) Check the voltage level of the signal between the signal high and signal ground. It cannot exceed the full scale range of the board.

3) Check other boards in your PC for address and interrupt conflicts.

4) Check that the CALL routine is in the QB4.5 directory where your BASIC program is.

5) Refer to the example programs for techniques and as a baseline to check code against.

PLEASE, NO RETURNS
WITHOUT RMA NUMBERS

Please, and here is why.

It slows down the solution of your problem.

If we receive a return without an RMA number written on the outside of the box, the contents of the box will sit in receiving until a Tech Support person is able to reach you and determine the reason for the return.

We need to know what you want us to look for.

The RMA system is fully automated and all the Tech Support engineers have access to the information in it. They can track your RMA and discuss your return history with you. This is very valuable if the setup you are using is overloading inputs. We can spot that and discuss a solution.
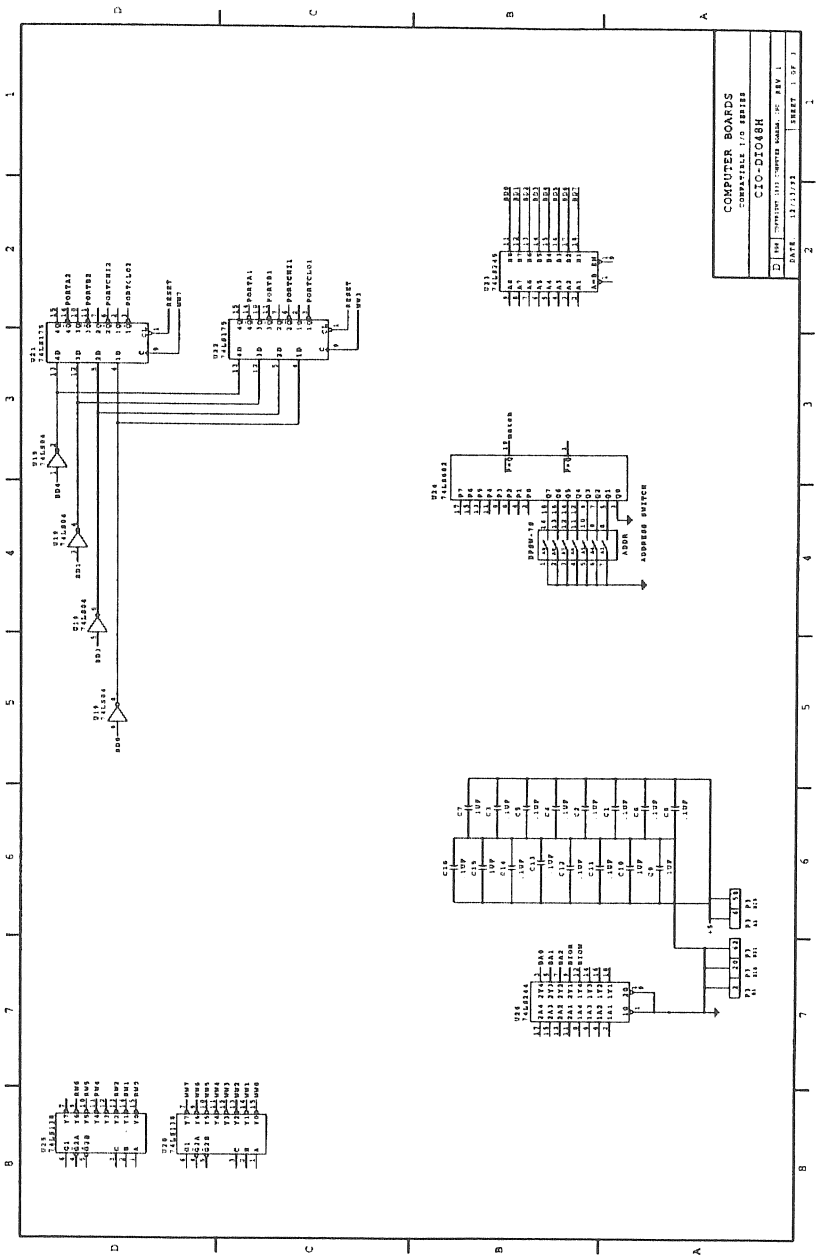
NOTATION:

This schematic shows the 82C55, connector and SIP arrangement for the CIO-DIO48 specifically. This configuration is consistent for the additional 82C55, connector and SIP combinations on the CIO-DIO96 and the CIO-DIO192.

COMPUTER BOARDS
COMPATIBLE I/O SERIES
CIO-DIO48/96/192

Page 21
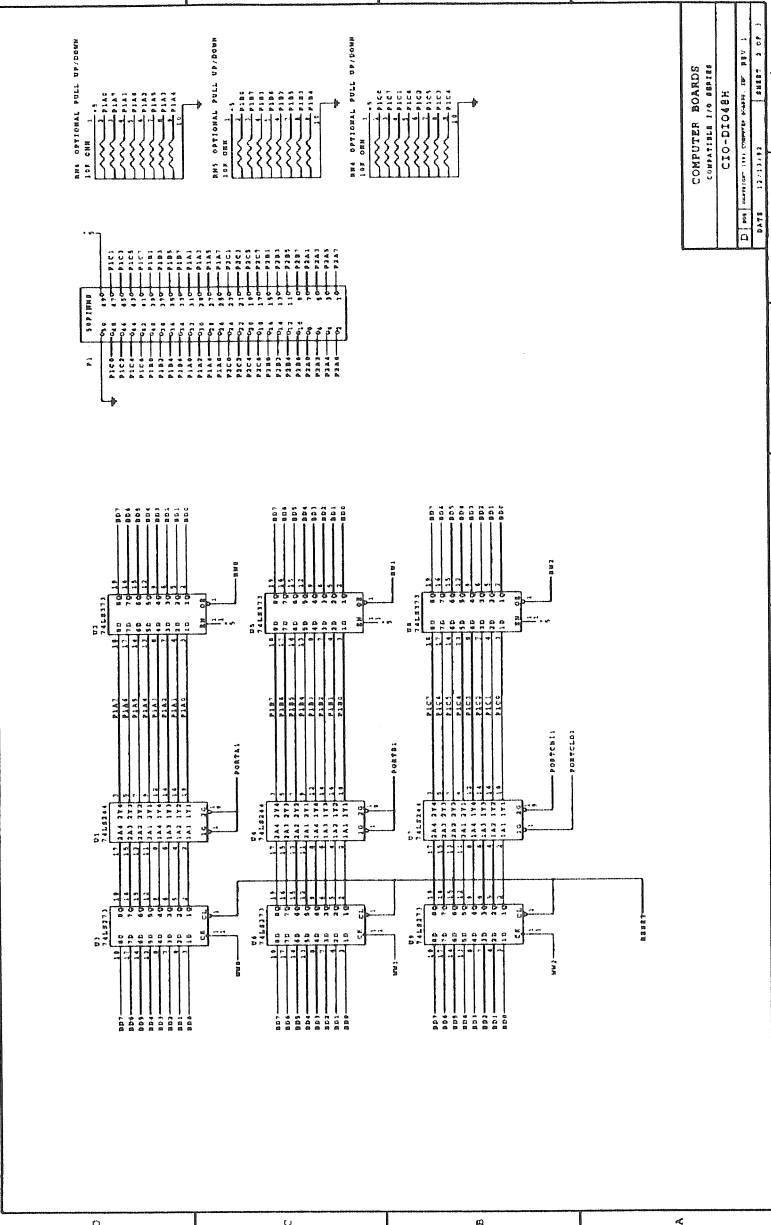
COMPUTER BOARDS
COMPATIBLE I/O SERIES
CIO-DIO48H
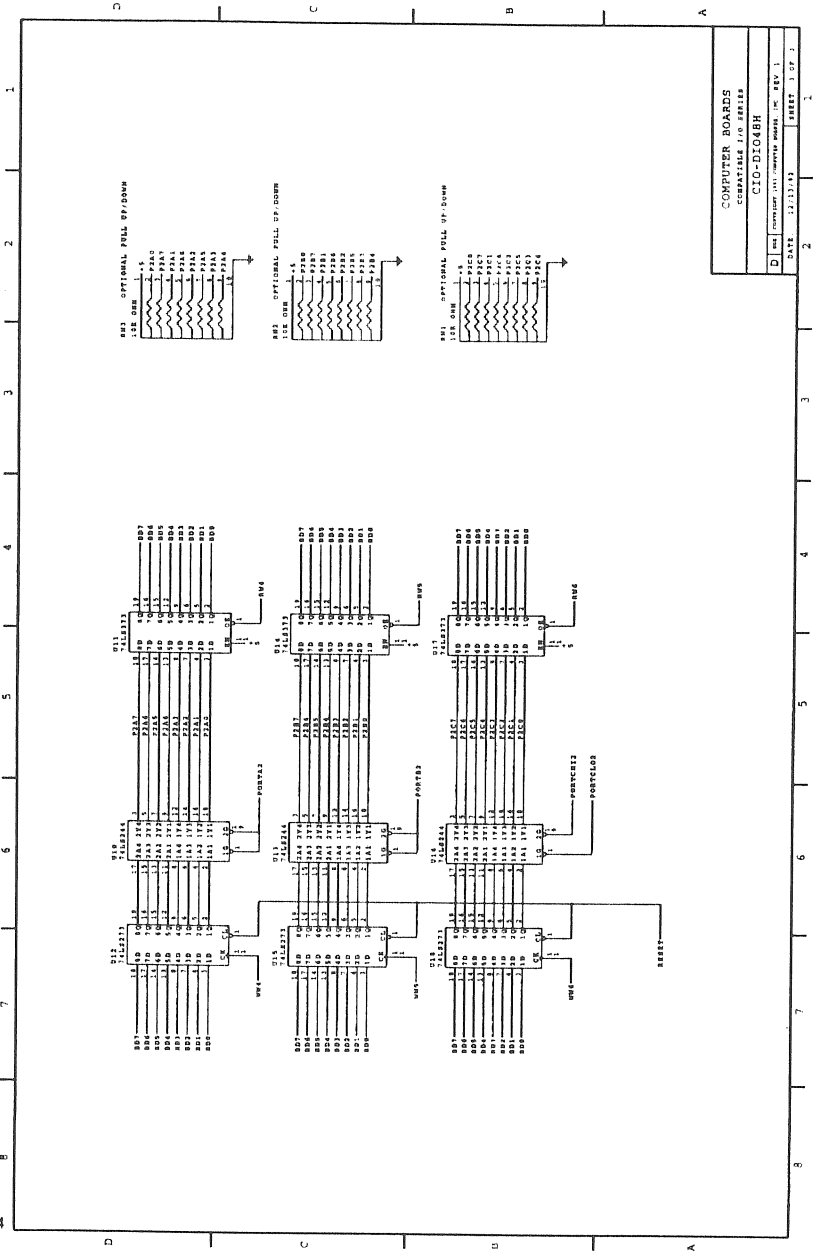
COMPUTER BOARDS
COMPATIBLE I/O SERIES
CIO-DIO48H

COMPUTER BOARDS
COMPATIBLE I/O SERIES
CIO-DIO48H

CIO-ERB24 COMPONENT LAYOUT

SCREW TERMINAL AND MODULE NUMBERS CORRESPOND TO 8255 PORTS AS:

1,2,3,4,5,6,7,8 = PORT A BITS 0,1,2,3,4,5,6,7
9,10,11,12,13,14,15,16 = PORT B BITS 0,1,2,3,4,5,6,7
17,18,19,20 = PORT C LOW, BITS 0,1,2,3
21,22,23,24 = PORT C HIGH, BITS 4,5,6,7

DUAL 50 PIN CONNECTORS
ALLOW CHAINING OF HIGH
DENSITY DIGITAL I/O BOARDS
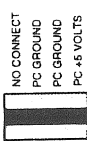
IN = CABLE FROM DIO BOARD
OUT = CABLE TO 2nd SSR-RACK24

D37 CONNECTOR
CONNECTS SIGNALS TO
DIGITAL I/O BOARD
INSIDE PERSONAL COMPUTER

NO CONNECT
PC GROUND
PC GROUND
PC +5 VOLTS

MOLEX TYPE CONNECTOR
MATES TO PC POWER
EXPANSION PLUG. INSIDE
PC.
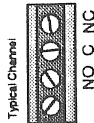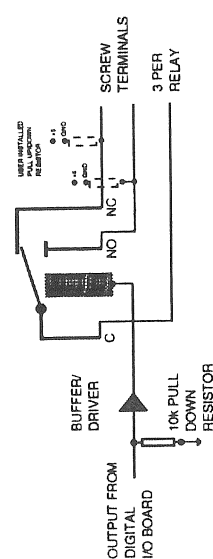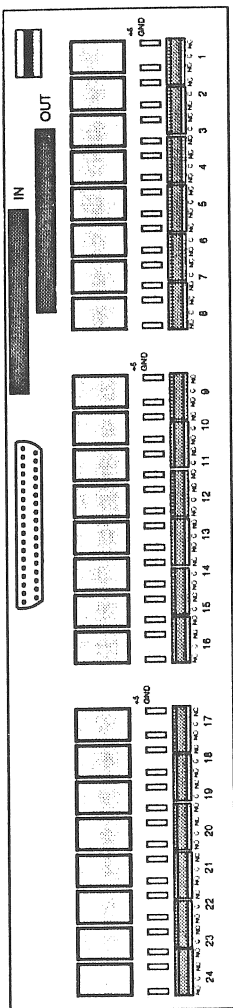
Typical Channel

NO   C   NC

C = COMMON
NC = NORMALL CLOSED, BIT = 0
     POWER OFF/ON STABLE STATE
NO = NORMALLY OPEN
     CLOSED WHEN BIT = 1

BUFFER/
DRIVER

OUTPUT FROM
DIGITAL
I/O BOARD

10k PULL
DOWN
RESISTOR

USER INSTALLED
PULL UP/DOWN
RESISTOR

SCREW
TERMINALS

3 PER
RELAY

SSR-RACK24 COMPONENT LAYOUT

NO CONNECT
PC GROUND
PC GROUND
PC +5 VOLTS

MOLEX TYPE CONNECTOR MATES TO PC POWER EXPANSION PLUG INSIDE PC.

SET PORT FOR INPUT MODULES
SET PORT FOR OUTPUT MODULES

PORT A CONTROL
PORT B CONTROL
PORT C HIGH 4 BITS CONTROL
PORT C LOW 4 BITS CONTROL

DUAL 50 PIN CONNECTORS ALLOW CHAINING OF HIGH DENSITY DIGITAL I/O BOARDS

IN = CABLE FROM DIO BOARD

OUT = CABLE TO 2nd SSR-RACK24

D37 CONNECTOR CONNECTS SIGNALS TO DIGITAL I/O BOARD INSIDE PERSONAL COMPUTER

IN

OUT

MOUNTING SCREW THREADS

Typical Channel

-2 +2 -1 +1

MODULE 2 NEGATIVE TERMINAL
MODULE 2 POSITIVE TERMINAL
MODULE 1 NEGATIVE TERMINAL
MODULE 1 POSITIVE TERMINAL

STATUS LED IS ON WHEN MODULE IS ACTIVE

SOCKETED POSITIONS FOR MODULES MANUFACTURED BY:
GORDOS, CRYDOM,
OPTO22, AND OTHERS.

SCREW TERMINAL AND MODULE NUMBERS CORRESPOND TO 8255 PORTS AS:

1,2,3,4,5,6,7,8 = PORT A BITS 0,1,2,3,4,5,6,7
9,10,11,12,13,14,15,16 = PORT B BITS 0,1,2,3,4,5,6,7
17,18,19,20 = PORT C LOW, BITS 0,1,2,3
21,22,23,24 = PORT C HIGH, BITS 4,5,6,7

CC
A B H L   OUT
IN

24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1

(C) COPYRIGHT COMPUTERBOARDS, INC. 1992

CIO-DIO48, 96 or 192

C50FF-2 CABLES

IN

OUT

RELAY BOARD

IN

SSR−RACK24 & CIO−ERB24
50 PIN CONNECTOR MARKED "IN"

Left label	Pin		Pin	Right label
GND	50	● ●	49	PIN 49 of 2nd CONNECTOR
RELAY 17	48	● ●	47	RELAY 18
RELAY 19	46	● ●	45	RELAY 20
RELAY 21	44	● ●	43	RELAY 22
RELAY 23	42	● ●	41	RELAY 24
RELAY 9	40	● ●	39	RELAY 10
RELAY 11	38	● ●	37	RELAY 12
RELAY 13	36	● ●	35	RELAY 14
RELAY 15	34	● ●	33	RELAY 16
RELAY 1	32	● ●	31	RELAY 2
RELAY 3	30	● ●	29	RELAY 4
RELAY 5	28	● ●	27	RELAY 6
RELAY 7	26	● ●	25	RELAY 8
2ND CONNECTOR PIN 48	24	● ●	23	2ND CONNECTOR PIN 47
2ND CONNECTOR PIN 46	22	● ●	21	2ND CONNECTOR PIN 45
2ND CONNECTOR PIN 44	20	● ●	19	2ND CONNECTOR PIN 43
2ND CONNECTOR PIN 42	18	● ●	17	2ND CONNECTOR PIN 41
2ND CONNECTOR PIN 40	16	● ●	15	2ND CONNECTOR PIN 39
2ND CONNECTOR PIN 38	14	● ●	13	2ND CONNECTOR PIN 37
2ND CONNECTOR PIN 36	12	● ●	11	2ND CONNECTOR PIN 35
2ND CONNECTOR PIN 34	10	● ●	9	2ND CONNECTOR PIN 33
2ND CONNECTOR PIN 32	8	● ●	7	2ND CONNECTOR PIN 31
2ND CONNECTOR PIN 30	6	● ●	5	2ND CONNECTOR PIN 29
2ND CONNECTOR PIN 28	4	● ●	3	2ND CONNECTOR PIN 27
2ND CONNECTOR PIN 26	2	● ●	1	2ND CONNECTOR PIN 25

2nd connector is marked "OUT" and is used to chain 24 of the 48 digital I/O to the second relay board.

BASE + 0, 8, 16, 24

GND	50	● ●	49	+5V
C0	48	● ●	47	C1
C2	46	● ●	45	C3
C4	44	● ●	43	C5
C6	42	● ●	41	C7
B0	40	● ●	39	B1
B2	38	● ●	37	B3
B4	36	● ●	35	B5
B6	34	● ●	33	B7
A0	32	● ●	31	A1
A2	30	● ●	29	A3
A4	28	● ●	27	A5
A6	26	● ●	25	A7

BASE + 4, 12, 20, 28

C0	24	● ●	23	C1
C2	22	● ●	21	C3
C4	20	● ●	19	C5
C6	18	● ●	17	C7
B0	16	● ●	15	B1
B2	14	● ●	13	B3
B4	12	● ●	11	B5
B6	10	● ●	9	B7
A0	8	● ●	7	A1
A2	6	● ●	5	A3
A4	4	● ●	3	A5
A6	2	● ●	1	A7

Address 300H shown

SW	HEX
A9	200
A8	100
A7	80
A6	40
A5	20
A4	10
A3	8
A2	4

9 8 7 6 5 4 3 2

↓ ↓ ↑ ↑ ↑ ↑ ↑ ↑

Wait State
Jumper Block

O O
N F
 F