DAC

CIO-DDA06

USER'S MANUAL

REVISION 2 April 1995

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1 INTRODUCTION

FACTORY DEFAULT BOARD SETUP: The CIO-DDA06 is setup at the factory with:

BASE ADDRESS	300H (768 Decimal) Same as data sheet.
WAIT STATE	Off position, Right.
SIMULTANEOUS UPDATE	In the XFER position. Single channel update.
ANALOG OUTPUT	±5V

2 SOFTWARE INSTALLATION

INSTALL PROGRAM

On the disk labeled InstaCal there is an installation program. Please run this program and accept the defaults. A new directory will be created on your hard disk and several lines will be added to AUTOEXEC and CONFIG files. If you have purchased the Universal Library for programming language support the installation program will prompt you for those disks also.

If you are installing Universal Library, please open the manual and read about the installation of that package.

Once all the software is installed, change to the CB directory and run InstaCal. Choose the INSTALL menu and select your board by part number from the list. Supply the information required for base address and any other switch set or programmable features. Heed and act upon any warning messages displayed.

You may then run TEST and test the installation of the board. Follow the instructions for signal connection displayed on the screen.

You may also run CALIBRATE and check the calibration of the board, although that is not necessary since the board was calibrated at the factory.

If you need it, there is some on-line help in the InstaCal program.

Owners of the Universal Library should read the manual and examine the example programs prior to attempting any programming tasks.

3 HARDWARE INSTALLATION

The CIO-DDA06 is a combination of 6 channels of analog output and a simple digital input and output board. The analog outputs are dual-DAC AD7273s with each output buffered by an OP07. The heart of the digital I/O is one 82C55. The CIO-DDA06 is 100% compatible with MetraByte's DDA-06.

The analog outputs are controlled by writing a digital control word as two bytes to the DAC's control register. The control register is double buffered so the DAC's output is not updated until both bytes (first low byte, then high byte) have been written to the DAC control.

The analog outputs may also be set for simultaneous update in groups of two, four or all six. Analog outputs are grouped as 0&1, 2&3 and 4&5. By selecting UPDATE on the jumper below the DAC, each pair may be set for simultaneous update.

When a DAC pair is set for simultaneous update, writing new digital values to the DAC's control register does *not* cause an update of the DAC's voltage output. Update of the output occurs only after a READ from the board's address (any address base + 0 through base + C).

In this way, the CIO-DDA06 may be set to hold new values until all channels are loaded, then update any two, four or all six channels simultaneously. This is a very handy feature for multi-axis motor control.

The CIO-DDA06 digital I/O lines are a direct interface to an 82C55. The 82C55 is a CMOS chip with TTL level inputs and outputs. The 8255 can sink about 8mA output low. This is more than enough to switch other TTL or similar inputs, but is inadequate for relays, LEDs or solid state relays.

The CIO-DDA06 digital I/O is controlled by programming the 8255's mode register. There are three possible modes. The simplest and most commonly used mode is mode 0, simple input and output.

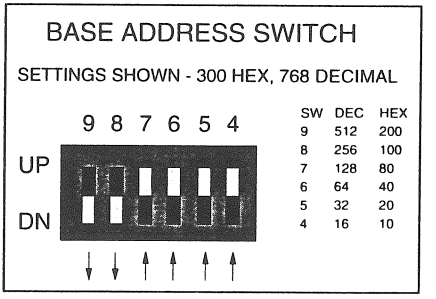
The CIO-DDA06 has one bank of gain switches, one base address switch, three simultaneous update jumpers and one wait state jumper block which must be set before installing the board in your computer. The calibration and test program included with the CIO-DDA06 will show how these switches are to be set and should be run before you open your computer.

3.1 BASE ADDRESS

The InstaCal program will request that you 'SELECT BASE ADDRESS', which allows you to choose a desired base address and adjusts the base address if necessary to place it on an 16 bit boundary.

After a base address is chosen, a diagram of the switch setting is drawn on the PC screen. Set the switches on your base address switch as shown on the diagram. Unless there is already a board in your system which uses address 300 HEX (768 Decimal) then you can leave the switches as they are set at the factory.

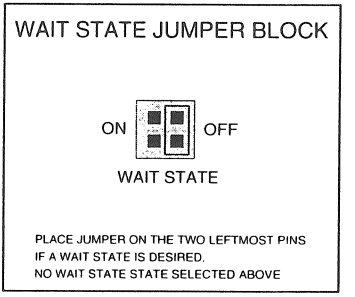
In the example shown here, the CIO-DDA06 is set for base address 300H (768 Decimal).



3.2 WAIT STATE JUMPER

The CIO-DDA06 boards have a wait state jumper which can enable an on-board wait state generator. A wait state is an extra delay injected into the processor's clock via the bus. This delay slows down the processor when the processor addresses the CIO-DDA06 board so that signals from slow devices (chips) will be valid.

The wait state generator on the CIO-DDA06 is only active when the CIO-DDA06 is being accessed. Your PC will not be slowed down in general by using the wait state.



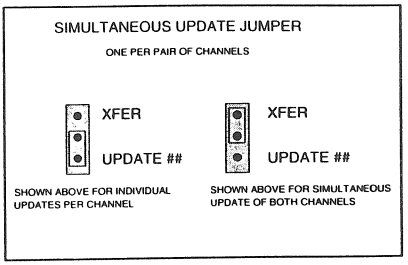
3.3 SIMULTANEOUS UPDATE JUMPER

The analog outputs may be jumpered so that new output data is held until several DACs have been loaded with new digital data, then, as a group, have that new data update the voltage outputs. The simultaneous update occurs whenever any of the CIO-DDA06 addresses BASE + 0 through BASE + C are read.

The analog output chips on the CIO-DDA06 are dual DACs. Two analog outputs are on each chip. A single jumper sets both DACs on a single chip to be simultaneous UPDATE or individual TRANSFER update.

The diagram to the right shows the jumper block in each configuration. If you look on the CIO-DDA06 board, you will see the numbers 45, 23 and 01 (left to right) next to the simultaneous update jumpers. Those number indicate which channels that jumper selects.

If you are familiar with the MetraByte DDA-06, you have probably noticed that only pairs, and not individual channels, may be selected for simultaneous update.



3.4 ANALOG OUTPUT RANGE SWITCH

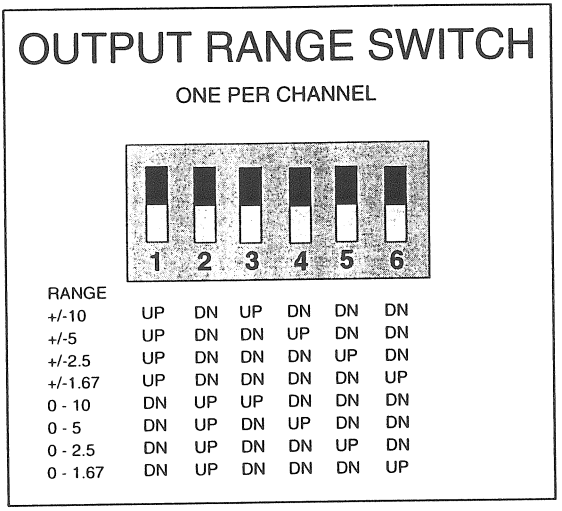
The analog output voltage range of each channel may be set via a six position DIP switch. The switches are located on the board directly below the calibration potentiometers and are labeled GAIN 5 through GAIN 0.

Set the switches for an individual channel as shown here.

To set in a chosen range, read the switch positions as Up or DN (down) from left to right in the row beside the range you desire.

For example, the ±5V range is: UP DN DN UP DN DN.

If you are familiar with the MetraByte DDA-06, you may have noticed that the CIO-DDA06 has more voltage ranges available but lack a 4-20mA output.



RANGE						
+/-10	UP	DN	UP	DN	DN	DN
+/-5	UP	DN	DN	UP	DN	DN
+/-2.5	UP	DN	DN	DN	UP	DN
+/-1.67	UP	DN	DN	DN	DN	UP
0 - 10	DN	UP	UP	DN	DN	DN
0 - 5	DN	UP	DN	UP	DN	DN
0 - 2.5	DN	UP	DN	DN	UP	DN
0 - 1.67	DN	UP	DN	DN	DN	UP

3.5 INSTALLING THE CIO-DDA06 IN THE COMPUTER

Turn the power off.

Remove the cover of you computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DDA06.

3.6 CABLING TO THE CIO-DDA06

The CIO-DDA06 connector is accessible through the PC/AT expansion bracket. The connector is a standard 37 pin male connector. A mating female connector may be purchased from Computer Boards, at Radio Shack or other electronic supply outlets.

Those familiar with MetraByte's DDA-06 will find the signal levels and pin assignments are identical with those on the CIO-DDA06. Those familiar with MetraByte's PIO12 and Computer Boards' CIO-DIO24, 24H and 48 will find the pin assignments of the 24 digital bits of those boards are identical with those on the CIO-DDA06

Several cabling and screw termination options are available from Computer Boards.

DFCON-37	D connector, D shell and termination pins to construct your own cable.
C37FF-2	2 foot (and longer) ribbon cable with 37 pin D connectors.
C37FFS-5	5 foot and 10 foot shielded round cable with molded ends housing 37 pin connectors. Also available 10 ft.
CIO-MINI37	Simple, 40 position 4"X4" screw terminal board.
CIO-TERMINAL	Full featured 4"X16" screw terminal board with prototyping and interface circuitry.
SSR-RACK24	24 position Solid State Relay mounting and interface board 5"X16".
ISO-RACK08	8 position Isolated Analog Module mounting and interface board.

3.7 SIGNAL CONNECTION TO TEST THE INSTALLATION

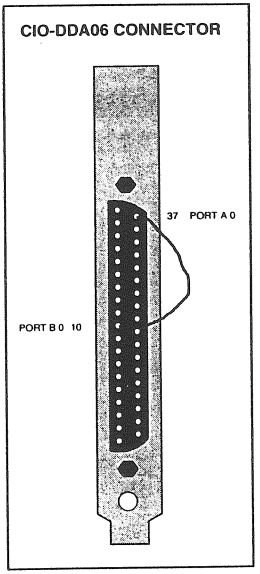
You may test the installation of the CIO-DDA06 using InstaCal TEST. The program allows you to set the DAC outputs and toggle the digital I/O. You will need a DVM to measure the voltage signals coming from the CIO-DDA06.

When testing digital inputs, please, before you connect a voltage from a signal generator or other source, be sure that the signal does not exceed 0-5V, the maximum digital input range.

The simplest test of the CIO-DDA06 is the program InstaCal TEST. This program toggles a digital output and reads a digital input and plots the digital level on the screen. This program requires a VGA type display.

Supplied with the CIO-DDA06 are some wires with plugs on each end. These are intended to be plugged directly on the CIO-DDA06 connector for loop-back testing. If you purchased a screw terminal then connect it up and use it instead.

To test the installation of the CIO-DDA06 the digital Output will be looped back into the digital input.



3.8 SIGNAL CONNECTION

The analog outputs of the CIO-DDA06 are two-wire hook-ups. A signal, labeled D/A # OUT on the connector diagram below, and a Low Level Ground (LLGND). The low level ground is an analog ground and is the ground reference which should be used for all analog hook-ups.

Possible analog output ranges are:

Bipolar Ranges	±10V	±5V	±2.5V	±1.67V
and Unipolar Ranges	0-10V	0-5V	0-2.5V	0.1.67V

See the range select switch in section 5.4

All the digital outputs inputs on the CIO-DDA06 connector are TTL level. TTL is an electronics industry term, short for Transistor Transistor Logic, which describes a standard for digital signals which are either at 0V or 5V. The binary logic inside the PC is all TTL or LSTTL (Low power Schotky TTL).

Under normal operating conditions, the voltages on the 8255 pins range from 0 to 0.45 volts for the low state to between 2.4 to 5.0 volts for the high state. At a voltage of 0.45 volts the 8255 can safely sink 2 mA. At a voltage of 2.4 volts the 8255 can source 0.4 mA. These values are typical of TTL devices.

The voltages and currents associated with external devices range from less than a hundred mA at a few volts for a small flash light bulb to 50 Amps at 220 volts for a large electric range. Attempting to connect either of these devices directly to the CIO-DDA06 would destroy the I/O chip.

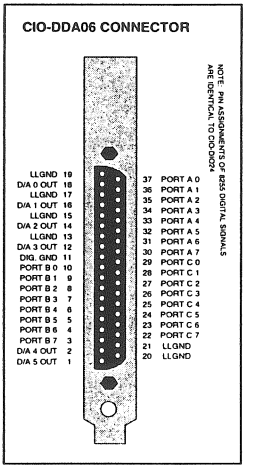
In addition to voltage and load matching, digital signal sources often need to be de-bounced. A complete discussion of digital interfacing will be found in the section on Interface Electronics in this manual.

3.9 CONNECTOR DIAGRAM

The CIO-DDA06 connector and the is a 37 pin D type connector accessible from the rear of the PC through the expansion backplate. The signals available are identical to those of MetraByte's DDA-06.

The connector accepts female 37 D type connectors, such as those on the C37FF-2, 2 foot cable with connectors.

If frequent changes to signal connections or signal conditioning is required, please refer to the information on the CIO-TERMINAL, CIO-SPADE50 and CIO-MINITERM screw terminal boards.



4 CALIBRATION

A calibration option is supplied with InstaCal.

The steps to calibrate the CIO-DDA06 are simple to follow. The are:

UNIPOLAR

1) To calibrate D/A 0, connect a DVM to analog output 0. The positive lead is connected to D/A 0 OUT, Pin 18. The ground lead is connected to LLGND, pin 19.

2) **OFFSET ADJUST**: Program the DAC with code=0. Adjust the offset potentiometer for a reading of 0.000 volts.

3) **GAIN ADJUST:** Program the DAC with code = 4095. Adjust the potentiometer for the full scale (FS) voltage - 1 LSB. For example, if you have set the D/A range switches for 0-10V, then (+FS - 1LSB) = (10 - 1LSB). One LSB equals the full scale range divided by 4095. In this case, 10/4095 = 0.00244. So, (10 - 0.00244) = 9.998V

4) Repeat the process above for the other DACs, 1-5

BIPOLAR

1) To calibrate D/A 0, connect a DVM to analog output 0. The positive lead is connected to D/A 0 OUT, Pin 18. The ground lead is connected to LLGND, pin 19.

2) **OFFSET ADJUST:** Program the DAC with code = 2048. Adjust the offset potentiometer for a reading of 0.000V on the DVM.

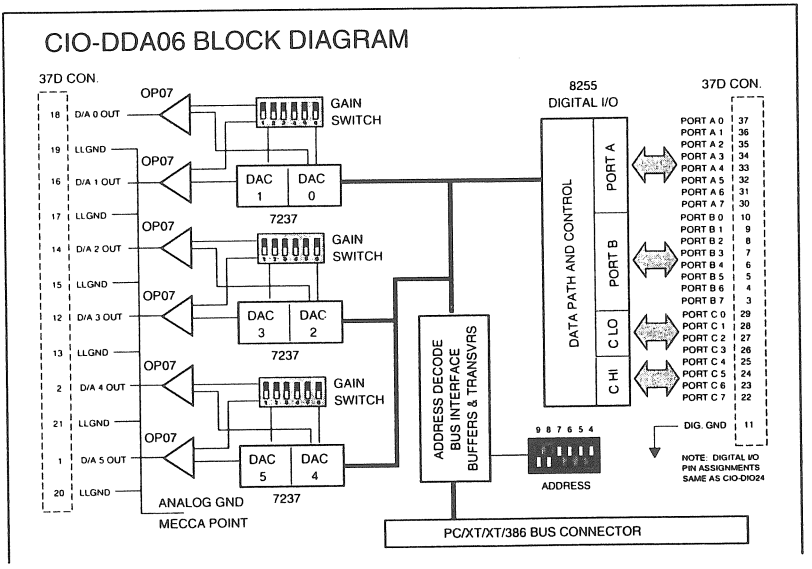
3) **GAIN ADJUST:** Program the DAC with code = 4095. Adjust the potentiometer for the positive full scale (+FS) voltage - 1 LSB. For example, if you have set the D/A range switches for ±5V, then (+FS - 1LSB) = (5 - 1LSB). One LSB equals the full scale range divided by 4095. In this case, 10/4095 = 0.00244. So, (5 - 0.00244) = 4.998V

4) Repeat the procedure for DACs 1-5.

5 ARCHITECTURE

The CIO-DDA06 is a simple board to understand right down to its lowest level. All control and data is read/written with simple I/O read and write signals. No interrupt or DMA control software is required. Hence, the board's functions are easy to control directly from BASIC, C or PASCAL.

Architecturally, the board may be viewed as two separate function blocks (see the block diagram below). The digital block consists of a single 82C55, 24 line digital I/O chip. The analog block consists of 3 identical circuits, each comprised of one dual DAC, two OP07 output buffers and range control. Each of the analog outputs may be individually controlled, or groups of 2, 4 or all 6 outputs may be controlled simultaneously.



5.1 CONTROL & DATA REGISTERS

The CIO-DDA06 has 12 analog output registers. There are two for each channel, one for the lower 8 bits and one for the upper 4 bits. An additional 4 address are occupied by the 82C55 data (3) and control (1) registers. The board occupies 16 I/O addresses in all.

The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

A register is easy to read and write to. Most often, register manipulation is best left to ASSEMBLY language programs as most of the CIO-DDA06 possible functions are implemented in an easy to use BASIC CALL.

The register descriptions all follow the format:

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write a control word or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

ADDRESS	WRITE FUNCTION	READ FUNCTION
BASE + 0	D/A 0 Least Significant Byte	Initiate simultaneous up.
BASE + 1	D/A 0 Most Significant Nibble	Initiate simultaneous up.
BASE + 2	D/A 1 Least Significant Byte	Initiate simultaneous up.
BASE + 3	D/A 1 Most Significant Nibble	Initiate simultaneous up.
BASE + 4	D/A 2 Least Significant Byte	Initiate simultaneous up.
BASE + 5	D/A 2 Most Significant Nibble	Initiate simultaneous up.
BASE + 6	D/A 3 Least Significant Byte	Initiate simultaneous up.
BASE + 7	D/A 3 Most Significant Nibble	Initiate simultaneous up.
BASE + 8	D/A 4 Least Significant Byte	Initiate simultaneous up.
BASE + 9	D/A 4 Most Significant Nibble	Initiate simultaneous up.
BASE + 10	D/A 5 Least Significant Byte	Initiate simultaneous up.
BASE + 11	D/A 5 Most Significant Nibble	Initiate simultaneous up.
BASE + 12	Port A Input of 8255	Port A Output of 8255
BASE + 13	Port B Input	Port B Output
BASE + 14	Port C Input	Port C Output
BASE + 15	None	Configure 8255

5.1.1 DIGITAL I/O REGISTERS

D/A 0 LEAST SIGNIFICANT 8 BITS
BASE ADDRESS + 0

300 HEX, 768 Decimal

7	6	5	4	3	2	1	0
D5	D6	D7	D8	D9	D10	D11	D12

D/A 0 MOST SIGNIFICANT 4 BITS
BASE ADDRESS + 1

301 HEX, 769 Decimal

7	6	5	4	3	2	1	0
X	X	X	X	D1	D2	D3	D4

Writing data to the LSB loads that data into the D/A load register but does not update the D/A output. Writing data to the MSB both loads the upper 4 bits of the 12 bit digital value and updates the output of the D/A.

The function and bit layout of the remaining 10 registers (5 D/As) is identical to that shown above.

PORT A DATA
BASE ADDRESS + 12

30C HEX, 780 Decimal

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0
Pin 30	Pin 31	Pin 32	Pin 33	Pin 34	Pin 35	Pin 36	Pin 37

PORT B DATA
BASE ADDRESS + 13 30D HEX, 781 Decimal

7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0
Pin 3	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10

Ports A & B may be programmed as input or output. Each is written to and read from in Bytes, although for control and monitoring purposes the individual bits are more interesting.

Bit set/reset and bit read functions require that unwanted bits be masked out of reads and ORed into writes.

PORT C DATA
BASE ADDRESS + 14 30E HEX, 782 Decimal

7	6	5	4	3	2	1	0
C8	C7	C6	C5	C4	C3	C2	C1
CH4	CH3	CH2	CH1	CL4	CL3	CL2	CL1
128 Bit	64 Weight	32 Dec.	16	8	4	2	1
80 Bit	40 Weight	20 HEX	10	8	4	2	1
Pin 21	Pin 23	Pin 24	Pin 25	Pin 26	Pin 27	Pin 28	Pin 29

Port C may be used as one 8 bit port of either input or output, or it may be split into two 4 bit ports which may be independently input or output. The notation for the upper 4 pit port is PCH3 - PCH0, and for the lower, PCL3 - PCL0.

Although it may be split, every read and write to port C carries 8 bits of data so unwanted information must be ANDed out of reads, and writes must be ORed with the current status of the other port.

OUTPUT PORTS

In 8255 mode 0 configuration, ports configured for output hold the output data written to them. This output byte may be read back by reading a port configured for output.

INPUT PORTS

In 8255 mode 0 configuration, ports configured for input read the state of the input lines at the moment the read is executed, transitions are not latched.

For information on modes 1 (strobed I/O) and 2 (bi-directional strobed I/O), you will need to acquire an Intel or AMD data book and see the 8255 data sheet.

8255 CONTROL REGISTER
BASE ADDRESS + 15 30F HEX, 783 Decimal

7	6	5	4	3	2	1	0
MS	M3	M2	A	CH	M1	B	CL
	Group A				Group B		

The 8255 may be programmed to operate in Input/ Output (mode 0), Strobed Input/ Output (mode 1) or Bi-Directional Bus (mode 2).

When the PC is powered up or RESET, the 8255 is reset. This places all 24 lines in Input mode and no further programming is needed to use the 24 lines as TTL inputs.

To program the 8255 for other modes, the following control code byte must be assembled into on 8 bit byte.

MS = Mode Set. 1 = mode set active

M3	M2	Group A Function	
0	0	Mode 0	Input / Output
0	1	Mode 1	Strobed Input / Output
1	X	Mode 2	Bi-Directional Bus

A	B	CL	CH	Independent Function
1	1	1	1	Input
0	0	0	0	Output

M1 = 0 is mode 0 for group B. Input / Output
M1 = 1 is mode 1 for group B. Strobed Input / Output

The Ports A, B, C High and C Low may be independently programmed for input or output.

The two groups of ports, group A and group B, may be independently programmed in one of several modes. The most commonly used mode is mode 0, input / output mode. The codes for programming the 8255 in this mode are shown below. D7 is always 1 and D6, D5 & D2 are always 0.

D4	D3	D1	D0	HEX	DEC	A	CU	B	CL
0	0	0	0	80	128	OUT	OUT	OUT	OUT
0	0	0	1	81	129	OUT	OUT	OUT	IN
0	0	1	0	82	130	OUT	OUT	IN	OUT
0	0	1	1	83	131	OUT	OUT	IN	IN
0	1	0	0	88	136	OUT	IN	OUT	OUT
0	1	0	1	89	137	OUT	IN	OUT	IN
0	1	1	0	8A	138	OUT	IN	IN	OUT
0	1	1	1	8B	139	OUT	IN	IN	IN
1	0	0	0	90	144	IN	OUT	OUT	OUT
1	0	0	1	91	145	IN	OUT	OUT	IN
1	0	1	0	92	146	IN	OUT	IN	OUT
1	0	1	1	93	147	IN	OUT	IN	IN
1	1	0	0	98	152	IN	IN	OUT	OUT
1	1	0	1	99	153	IN	IN	OUT	IN
1	1	1	0	9A	154	IN	IN	IN	OUT
1	1	1	1	9B	155	IN	IN	IN	IN

5.2 PC/XT/AT BUS INTERFACE

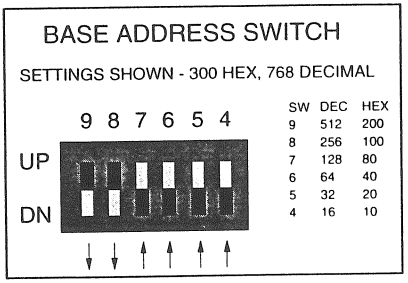
The CIO-DDA06 employs the PC bus for power, communications and data transfer. As such it draws power from the PC, monitors the address lines and control signals and responds to it's I/O address, and it receives and places data on the 8 data lines.

The BASE address is the most important user selectable bus related feature of the CIO-DDA06. The base address is the location that software writes to and reads from when communicating with the CIO-DDA06.

The base address switch is the means for setting the base address. Each switch position corresponds to one of the PC bus address lines. By placing the switch down, the CIO-DDA06 address decode logic is instructed to respond to that address bit.

A complete address is constructed by calculating the HEX or decimal number which corresponds to all the address bits the CIO-DDA06 has been instructed to respond to. For example, shown to the right are address 9 and 8 down, all others up.

Address 9 = 200H (512D) and address 8 = 100H (256D), when added together they equal 300H (768D).



Certain address are used by the PC, others are free and may be used by the CIO-DDA06 and other expansion boards. We recommend BASE = 300H (768D) be tried first.

TABLE OF I/O ADDRESS

HEX RANGE	FUNCTION
000-00F	8237 DMA #1
020-021	8259 PIC #1
040-043	8253 TIMER
060-063	8255 PPI (XT)
060-064	8742 CONTROLLER (AT)
070-071	CMOS RAM & NMI MASK (AT)
080-08F	DMA PAGE REGISTERS
0A0-0A1	8259 PIC #2 (AT)
0A0-0AF	NMI MASK (XT)
0C0-0DF	8237 #2 (AT)
0F0-0FF	80287 NUMERIC CO-P (AT)
1F0-1FF	HARD DISK (AT)
200-20F	GAME CONTROL
210-21F	EXPANSION UNIT (XT)
238-23B	BUS MOUSE
23C-23F	ALT BUS MOUSE
270-27F	PARALLEL PRINTER
2B0-2BF	EGA

HEX RANGE	FUNCTION
2C0-2CF	EGA
2D0-2DF	EGA
2E0-2E7	GPIB (AT)
2E8-2EF	SERIAL PORT
2F8-2FF	SERIAL PORT
300-30F	PROTOTYPE CARD
310-31F	PROTOTYPE CARD
320-32F	HARD DISK (XT)
378-37F	PARALLEL PRINTER
380-38F	SDLC
3A0-3AF	SDLC
3B0-3BB	MDA
3BC-3BF	PARALLEL PRINTER
3C0-3CF	EGA
3D0-3DF	CGA
3E8-3EF	SERIAL PORT
3F0-3F7	FLOPPY DISK
3F8-3FF	SERIAL PORT

The CIO-DDA06 BASE switch may be set for address in the range of 000-3F0 so it should not be hard to find a free address area for you CIO-DDA06. Once again, if you are not using IBM prototyping cards or some other board which occupies these addresses, then 300-31F HEX are free to use.

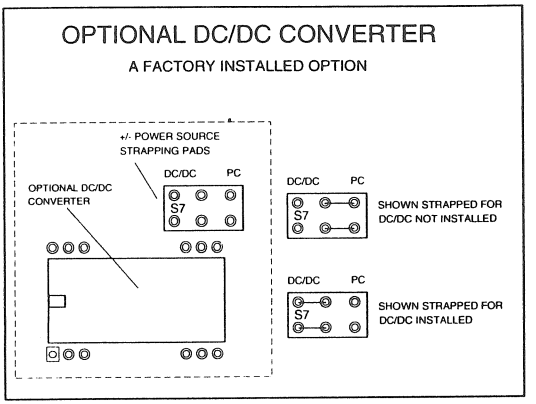
Address not specifically listed, such as 390-39F, are free.

5.3 OPTIONAL DC/DC CONVERTER

An optional DC/DC converter may be installed by Computer Boards. The DC/DC converter provides ±15V, eliminating the need for the ±12V supply of the PC.

This option is useful only to those who wish to install the CIO-DDA06 in a PC that does not have both ±12V, such as a portable.

This $30 option must be specified at the time of order by adding a CIO-PG408 to the order.



6 SPECIFICATIONS

6.1 POWER CONSUMPTION

CIO-DDA06

+5V Supply	435 mA typical / 525 mA max.
+12V Supply	50mA typical / 80 mA max.
-12V Supply	120 mA typical / 160 mA max

CIO-DDA06 WITH DC/DC INSTALLED

+5V Supply	935 mA typical / 1.025A max.

ANALOG OUTPUTS

Channels	6
Resolution	12 bits (1 part in 4095)
D/A type	Dual DAC, AD7237
Latches	Double buffered w/ optional sim. update.
Linearity	± 1/2 bit
Monotonicity	± 1/2 bit
Temperature drift	1 ppM typical, 3 ppM max @ 0 15 ppM typical, 30 ppM max @ full scale gain.
Output ranges	0 to 10 volts 0 to 5 volts 0 to 2.5 volts 0 to 1.67 volts ±10 volts ±5 volts ±2.5 volts ±1.67 volts

Load current	±5mA max
Short circuit current	40mA max
Output resistance	<0.1 ohm
Settling time +FS 0.01%	3uS typical, 5uS max
Settling time -FS 0.01%	5uS typical, 10uS max

6.2 DIGITAL I/O

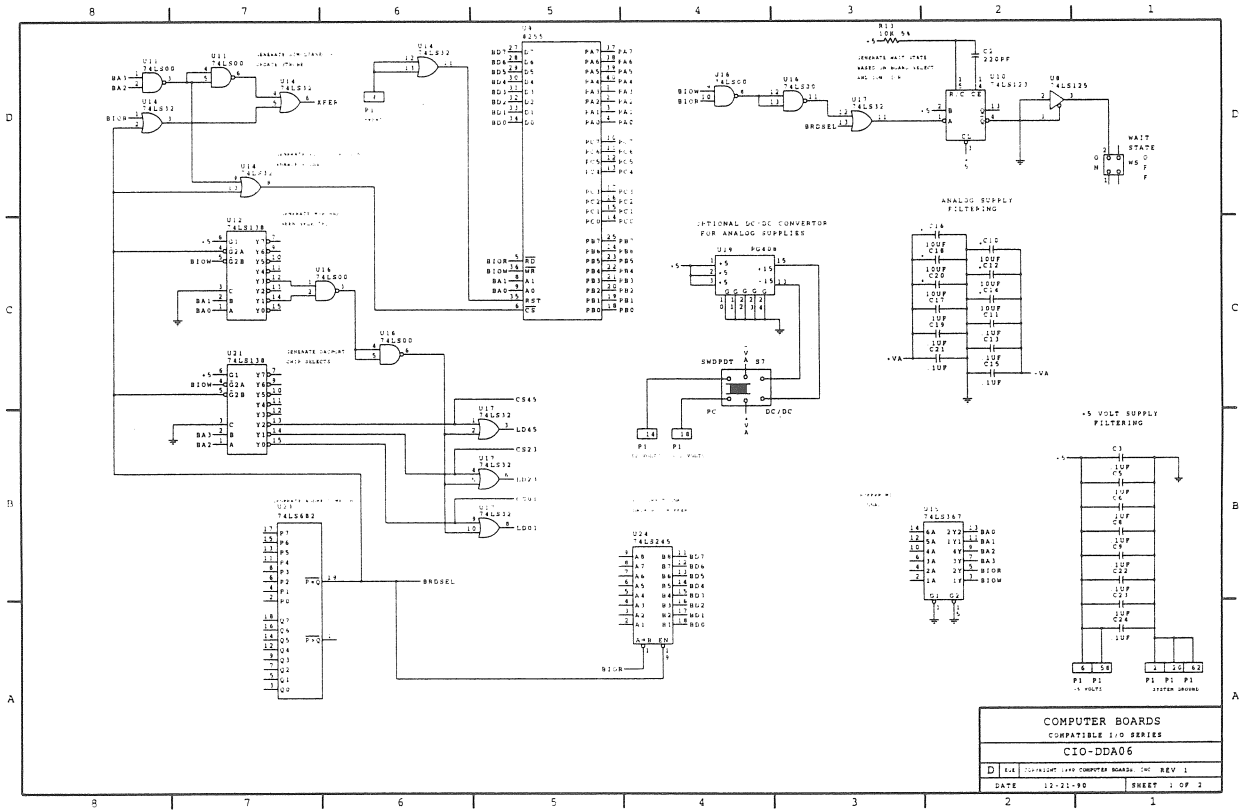
TTL LEVEL DIRECT TO/FROM 8255 CHIPS

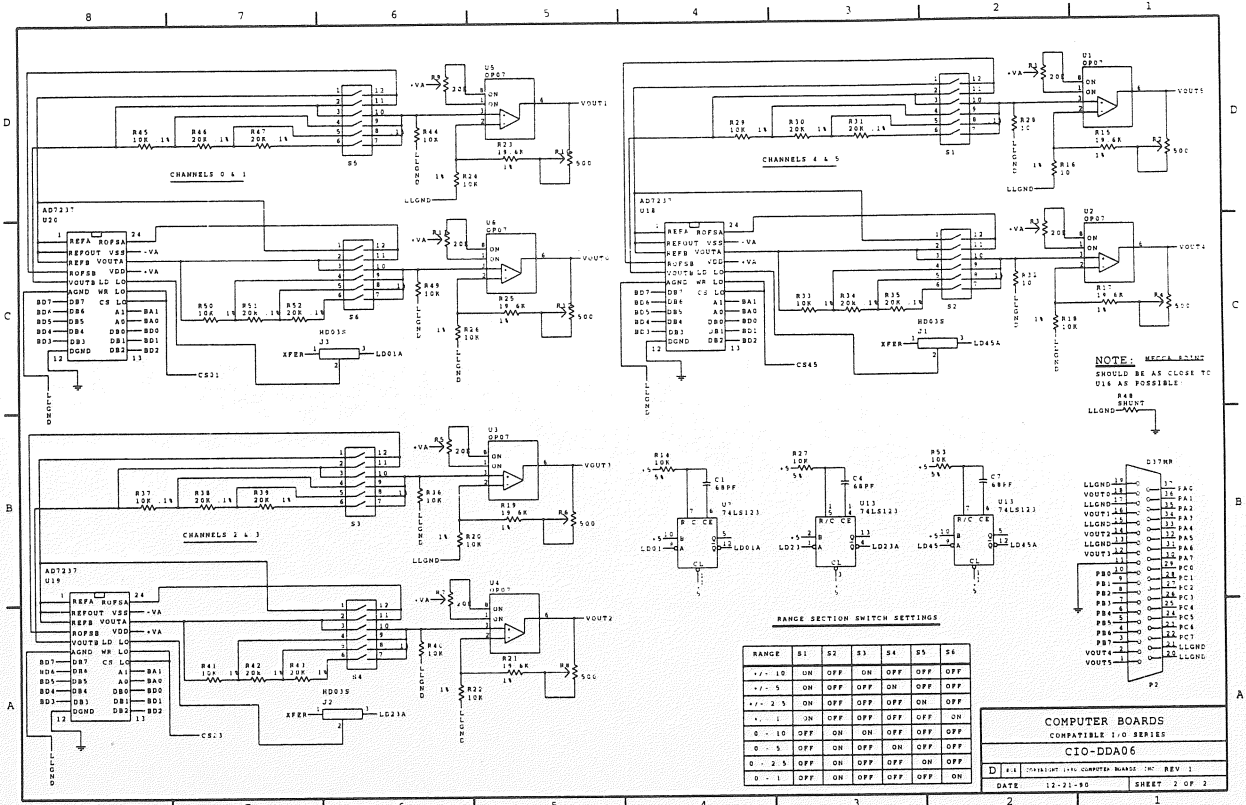
8255 output high	2.4 V min @ -200 uA
8255 output low	0.5 V max @ 2.5 mA
8255 input high	2.0 V min, 7 V max
8255 input low	-0.5 V min, 0.8 V max
8255 drive capability	5 LSTTL loads

6.3 ENVIRONMENTAL

Operating Temperature	0 - 50 deg C
Storage Temperature	-20 to 70 deg C
Humidity	0 to 90% non-condensing
Weight	6.35 oz

7 Schematics


U9
8255
U11
74LS00
U14
74LS32
U12
74LS138
U16
74LS00
U21
74LS138
U23
74LS682
U24
74LS245
U15
74LS367
U18
74LS00
U17
74LS32
U10
74LS123
U8
74LS125
R33
10K 5%
C2
220PF
WAIT STATE
OPTIONAL DC-DC CONVERTOR FOR ANALOG SUPPLIES
U19 PG40W
SWDPDT
ANALOG SUPPLY FILTERING
+5 VOLT SUPPLY FILTERING
BRDSEL
BIOR
BIOW
CS45
CS21
LD45
LD21
LD01
COMPUTER BOARDS
COMPATIBLE I/O SERIES
CIO-DDA06
DATE 12-21-90
SHEET 1 OF 2


CHANNELS 0 & 1
CHANNELS 4 & 5
CHANNELS 2 & 3
AD7237
U20
U18
U19
HD0038
XFER
CS21
CS45
CS3
LD01A
LD45A
LD23A
LD01
LD23
LD45
VOUT0
VOUT1
VOUT2
VOUT3
VOUT4
VOUT5
+VA
-VA
LLGND
DGND
NOTE: REFCA POINT SHOULD BE AS CLOSE TO U16 AS POSSIBLE.
R48 SHUNT
D37MP
P2
RANGE SECTION SWITCH SETTINGS
RANGE | S1 | S2 | S3 | S4 | S5 | S6
+/- 10 | ON | OFF | ON | OFF | OFF | OFF
+/- 5 | ON | OFF | OFF | ON | OFF | OFF
+/- 2.5 | ON | OFF | OFF | OFF | ON | OFF
+/- 1 | ON | OFF | OFF | OFF | OFF | ON
0 - 10 | OFF | ON | ON | OFF | OFF | OFF
0 - 5 | OFF | ON | OFF | ON | OFF | OFF
0 - 2.5 | OFF | ON | OFF | OFF | ON | OFF
0 - 1 | OFF | ON | OFF | OFF | OFF | ON
COMPUTER BOARDS
COMPATIBLE I/O SERIES
CIO-DDA06
D
DATE 12-21-90
SHEET 2 OF 2