ADC

CIO-DAS48-PGA

USER'S MANUAL

REVISION 1, January 1993

&

DAS48 UTILITY DISK

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1 INTRODUCTION

This manual is intended to assist your application of the CIO-DAS48-PGA to your measurement or control problem. We are interested in your corrections and suggestions. There is no mail-in suggestion form in this manual because we would prefer to talk to you. Please pick up the phone and speak with one of our Technical Support/Sales Engineers. They will note all of your suggestions for implementation in the next revision of this manual.

As a CIO-AD board owner, the latest manual revision is yours free, any time you request it.

ORGANIZATION

This manual is organized in the order that you are likely to need the information in it. To fully understand the CIO-DAS48-PGA and the implications of installing and using it, we suggest that you read the manual and follow along. It will take only an hour or so and when you have finished you will be prepared to use your CIO-DAS48-PGA.

INSTALLATION	How to install the CIO-DAS48-PGA.
SOFTWARE	How to install and run the supplied software.
CALIBRATION	How to calibrate and test the board.
SIGNAL CONNECTION	How to connect analog signals.
PROGRAMMING	How to program the CIO-DAS48 from Basic.
ARCHITECTURE	How the board works and how to program the registers.
ANALOG ELECTRONICS	A *very* basic course in the subject.
PC ARCHITECTURE	How the architecture of the PC affects board performance.
DIAGNOSIS & DEBUG	What to do if you think the board is broken.

2 INSTALLATION

The CIO-DAS48-PGA board is an extension of the popular CIO-DAS08 architecture. The channels have been expanded to 48 single enede inputs or 24 differential inputs. The 24 Differential inputs may be adapted for current measurements.

1) Gains are software programmable. There is only one version of the CIO-DAS48-PGA with gains of 0.5, 1, 2, 4 and 8.
2) Analog inputs are differential(24) or single ended (48). In differential mode, an optional 10K SIP provides ground reference to the CH LO inputs. These may be installed in banks of 8.
3) A current measurement conversion kit contains 6 SIP resistors which when installed on the CIO-DAS48-PGA, convert the 24 differential voltage measurements inputs into 24 current measurements inputs. The current measurement resistor kit is not provided with the CIO-DAS48-PGA. This kit is included with your CIO-DAS48-PGA. The part number is CIO-DAS48-ISIP
4) A DC/DC converter supplies stable ±15V power to the analog circuitry. It is possible to construct the board without the DC/DC converter. This saves money (reduces your cost) but does limit the ranges of analog input and is available only to orders of 10 or more units.

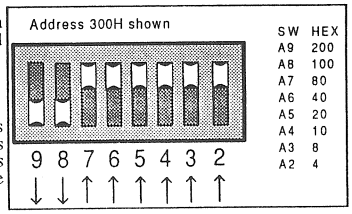
The CIO-DAS48-PGA has one bank of switches, the Base Address Switch, which must be set before installing the board in your computer.

2.1 BASE ADDRESS

The base address of the CIO-DAS48-PGA is set by switching a bank of DIP switches on the board. This bank of switches is labeled ADDRESS and numbered 9 to 2.

Ignore the word ON and the numbers printed on the switch

The switch works by adding up the weights of individual switches to make a base address. A 'weight' is active when the switch is down. Shown to the right, switches 9 and 8 are down, all others are up. Weights 200H and 100H are active, equaling 300H base address.



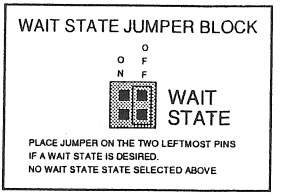
The CIO-DAS48-PGA occupies 4 I/O locations. A table of the ports and functions below is explained elsewhere in this manual, in detail.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 - 12(LSB)	Start 8 bit A/D conversion
BASE + 1	A/D Bits 1(MSB) - 8	Start 12 bit A/D conversion
BASE + 2	EOC, Current MUX Address	Set MUX address
BASE + 3	Gain/range, DIFF/SINGLE switch.	Set gain/range

2.2 WAIT STATE

A wait state may be enabled on the CIO-DAS48-PGA by selecting WAIT STATE ON at the jumper provided on the board. Enabling the wait state causes the personal computer's bus transfer rate to slow down whenever the CIO-DAS48-PGA is written to or read from.

The wait state jumper is provided in case you one day own a personal computer with an I/O bus transfer rate which is too fast for the CIO-DAS48-PGA. If your board were to fail sporadically in random ways, you could try using it with the wait state ON.



2.3 MODE V-I JUMPER

The jumper labeled MODE V-I must be set to match the type of input, voltage(V) or current(I).

Only move the jumper from V to I if you have installed the CIO-DAS48-ISIP kit.

2.4 CURRENT LOOP MEASUREMENTS

Before current loop measurements are made, the resistor SIP kit, CIO-DAS48-ISIP must be installed. Once installed, the inputs of the CIO-DAS48-PGA are committed to current measurement and may no longer be used for voltage measurement.

The SIPs RN7, RN8 and RN9 must not be installed if the board is to be used for current measurement. Or, if previously installed, must be removed.

Removal of the ISIPs restores the CIO-DAS48-PGA the inputs to voltage measurement. Removal must be done by clipping off the SIPs. If you want to de-solder the SIPs the board must be returned to the factory.

It is not possible to install only a portion of the ISIPs and have a mixture of current and voltage inputs. You must install all 6 SIPs from the CIO-DAS48-ISIP package and set the MODE V-I jumper to I. ISIPs are installed in RN1, RN2, RN3, RN4, RN5, and RN6.

NOTE: *Special instructions and solder are packaged with the CIO-DAS48-ISIP kit. Follow the installation instructions carefully and use the solder provided. Use of other solder, or failure to follow instructions will probably result in a degradation of the analog input's accuracy and will require out-of-warranty repair.*

NOTE: The selection of the ISIPs is critical. Variations in either value or tolerance from those supplied in the CIO-DAS48-ISIP will result in measurement inaccuracy.

2.5 INSTALLING THE CIO-DAS48-PGA IN THE COMPUTER

Turn the power off.

Remove the cover of your computer. Please be careful not to dislodge any of the cables installed on the boards in your computer as you slide the cover off.

Locate an empty expansion slot in your computer.

Push the board firmly down into the expansion bus connector. If it is not seated fully it may fail to work and could short circuit the PC bus power onto a PC bus signal. This could damage the motherboard in your PC as well as the CIO-DAS48-PGA.

2.6 SIGNAL CONNECTION TO TEST THE INSTALLATION

To test the installation of the CIO-DAS48-PGA there must be electrical signals for it to read and display. You must supply the signal with a function generator or other voltage or current source.

Please, before you connect a voltage from a signal generator or other source, be sure that the signal does not exceed +/- 10V, the maximum analog input range of the board, or 20mA, the maximum current input range. The analog inputs are protected to 30V but why prove it.

Use the progran IOTEST.EXE.

Mode	Connections
48 Single	Pin 1 to signal high Pin 49 to signal low
24 Differential	Pin 1 to Signal high Pin 2 to signal low Pin 49 to signal source ground.
24 4-20mA Current	Pin 1 to + current Pin 2 to - current

3 SOFTWARE

The software supplied with the CIO-DAS48-PGA consists of BASIC examples, including calibration and test programs are on the disk marked CIO-DAS48-PGA UTILITY PROGRAMS.

There is no CALL routine and no Acquire or Lablog2 software supplied with the CIO-DAS48.

The programming examples show how to program the gain register, set the channel mux, trigger a conversion and read the conversion results. Because the CIO-DAS48-PGA has no interrupt or DMA capability is is very easy to program directly; no CALL routine or library is needed.

The examples provided on disk should get you started programming the board. For more information, refer to the section onm the registers and their functions.

4 CALIBRATION AND TEST

The CIO-DAS48-PGA is supplied with software for calibration and test.

4.1 FREQUENCY OF CALIBRATION

Every board was fully tested and calibrated before being placed in finished goods inventory at the factory. For normal environments a calibration interval of 6 months to one year is recommended. If frequent variations in temperature or humidity are common then re-calibrate at least once every three months. It takes less than 30 minutes to calibrate the CIO-DAS48-PGA.

If you install the CIO-DAS48-ISIP kit for current measurement, you will need to re-calibrate the board.

4.2 REQUIRED EQUIPMENT

Ideally, you will need a precision voltage source and some pieces of wire. If you do not have a precision voltage source, you will need a non-precision source, a 4 1/2 digit digital volt meter, a calculator and have to make a few calculations.

You will not need an extender card to calibrate the board but you will need to have the cover off you computer with the power on, so trimpots can be adjusted during calibration. For that reason a plastic screwdriver has been supplied with your CIO-DAS48-PGA. In the event that the screwdriver is dropped into the PC, no damage will result from short circuits.

4.3 CALIBRATING THE ANALOG INPUTS

There are two different calibration procedures. One for voltage input, the other is for current input. Your CIO-DAS48-PGA is in current input ONLY if you have installed the current input conversion kit, CIO-DAS48-ISIP

Complete calibration software is included on the CIO-DAS48-PGA utility disk. This software is designed for the CIO-DAS48-PGA and explains the connections and signals required for complete calibration. The program is called CAL48PGA.EXE.

The CIO-DAS48-PGA will not require recalibration when moved from one personal computer to another. The reason is that the CIO-DAS48-PGA has a stable DC/DC converter on-board which supplies the analog ±15V voltages.

Here is the calibration sequence which the calibration software steps you through.

CALIBRATION - VOLTAGE INPUT

The CIO-DAS48-PGA is supplied from the factory in voltage input mode. This calibration procedure requires the CIO-DAS48-PGA to be in 48 channel single ended input mode.

If you have installed the SIP resistors RN7 - RN9 to provide a reference to ground for the differential input low channels, the CIO-DAS48-PGA will only operate in 24 channel differential input mode but it should be calibrated with the DIFF-SINGLE switch in the SINGLE position.

PLEASE SEE THE SECTION ON INSTALLING SIP RESISTORS FOR CAUTIONS.

The following calibration procedure applies to 24 DIFF and 48 SINGLE modes.

1) DIFFERENCE AMPLIFIER NULLING
   - Set DIFF - SINGLE switch to SINGLE
   - Place MODE V-I jumper to V
   - Short pins 1 and 49
   - Program range to ±5V (code = 0)
   - Adjust Amp Out Offset potentiometer (R10) until the board reads 0 counts.
   - Program range to ±0.625V (code = 6)
   - Adjust Amp In Offset pot (R11) until the board reads 0 counts

2) UNIPOLAR OFFSET ADJUSTMENT
   - Program range to 0-10V (code = 1)
   - Adjust Unipolar Offset pot (R16) until the board reads 0/1 counts.

3) BIPOLAR OFFSET ADJUSTMENT
   - Apply -4.998V between pins 1 an 49
   - Program range to ±5V (code = 0)
   - Adjust Bipolar Offset (R15) pot until board reads -2047/-2048 counts.

4) GAIN ADJUSTMENT
   - Apply +4.998V between pins 1 and 49
   - Program range to ±5V (code = 0)
   - Adjust A/D Gain pot (R14) until the board reads 2046/2047 counts.

CALIBRATION - CURRENT INPUT

The CIO-DAS48-PGA is supplied from the factory in voltage input mode. This calibration procedure requires the CIO-DAS48-ISIP kit to be installed and the board converted to current measurement mode.

If you have installed the SIP resistors RN1 - RN6 to accept current inputs, the CIO-DAS48-PGA will only operate in 24 channel current input mode and it should be calibrated with the DIFF-SINGLE switch in the DIFF position.

PLEASE SEE THE SECTION ON INSTALLING SIP RESISTORS FOR CAUTIONS.

The following calibration procedure applies to 24 DIFF (current) mode only.

CURRENT INPUT CALIBRATION USING A PRECISION VOLTAGE SOURCE.

Note: Voltage source must be able to supply 2.000 volts at 20mA or greater.

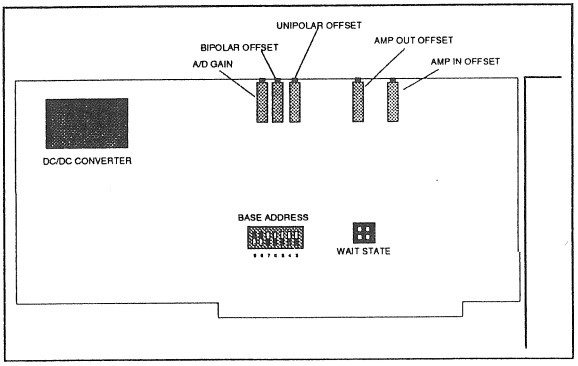
1) DIFFERENCE AMPLIFIER NULLING
   - Set DIFF - SINGLE switch to DIFF
   - Place MODE V-I jumper to I
   - Connect 400mV between pins 1 (+ source) and 49 (- source).
   - Program range to 0-10V (code = 1)
   - Adjust Amp Out Offset potentiometer (R10) until the board reads 0 counts. This is a coarse adjustment.
   - Apply 4.002mA between pin 1 and pin 49.
   - Adjust Amp In Offset pot (R16) until the board reads 0/1 counts. This is a fine adjustment.

2) GAIN ADJUSTMENT
   - Apply +1.9994V between pins 1 and 49
   - Program range to 0-10V (code = 1)
   - Adjust A/D Gain pot (R14) until the board reads 4096/4095 counts.

CURRENT INPUT CALIBRATION USING A PRECISION CURRENT SOURCE.

1) DIFFERENCE AMPLIFIER NULLING
   - Set DIFF - SINGLE switch to DIFF
   - Place MODE V-I jumper to I
   - Apply 4mA between pins 1 (+ source) and 49 (- source).
   - Program range to 0-10V (code = 1)
   - Adjust Amp Out Offset potentiometer (R10) until the board reads 0 counts. This is a coarse adjustment.
   - Apply 400.2mV between pin 1 and pin 49.
   - Adjust Amp In Offset pot (R16) until the board reads 0/1 counts. This is a fine adjustment.

2) GAIN ADJUSTMENT
   - Apply 19.994mA between pins 1 and 49
   - Program range to 0-10V (code = 1)
   - Adjust A/D Gain pot (R14) until the board reads 4096/4095 counts.



5 SIGNAL CONNECTION

Signal connection can be one of the most challenging aspects of applying a data acquisition board. If you are an *Analog* Electrical Engineer then this section is not for you, but if you are like most PC data acquisition people these simple examples should get you started. The objective here is to present 'how to connect' common signals while avoiding discussion of electrical theory and special symbols. If you need a connection we do not show, or if you invent one, please call and tell us so we can add it to this manual.

5.1 CONNECTOR DIAGRAM

The connector pin names CH 0 HI through CH 47 HI reflect the single ended configuration of the CIO-DAS48-PGA inputs.

The connector pin names CH 0 LOW & HI through CH 23 LOW & HI reflect the differential configuration of the CIO-DAS48-PGA inputs.

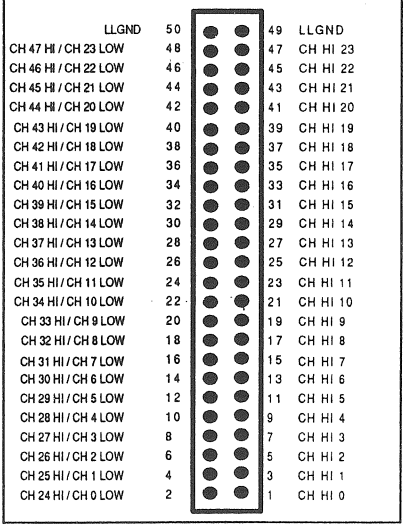
Current connections are made between CH# HI and CH# LOW. The +current must be connected to CH# HI.

The CIO-DAS48-PGA analog connector is a 50 pin header type connector accessible from the rear of the PC through the expansion backplate.

The connector accepts female 50 pin header connectors, such as those on the C50FF-2, 2 foot cable with connectors.

If frequent changes to signal connections, please refer to the information on the CIO-MINI50 in the ComputerBoards catalog.

View From Component Side of Board



5.2 SINGLE ENDED INPUTS

Single ended inputs are two wire connections between the signal source and the A/D board. A single wire carries the signal, and is connected from the signal source to Channel ## HI. The ground from the signal source must be connected to LLGND, pins 49 or 50.

5.3 DIFFERENTIAL INPUTS

The CIO-DAS48-PGA can have differential analog inputs. For a complete discussion of differential vs. single ended analog inputs, turn to the section of this manual on Analog Electronics; the subsection on that subject.

Briefly, differential inputs are 3 wire analog hookups consisting of a signal high, signal low and chassis ground. The signal source high is connected to Channel N HI, the signal source low is connected to Channel N LOW, the signal source GND is connected to LLGND

The benefits of differential inputs are the ability to reject noise which affects both signal high and low, and the ability to compensate for ground loops or potentials between signal low and chassis ground.

5.4 PSEUDO DIFFERENTIAL

Modified differential inputs provide much of the environmental-noise immunity and common mode rejection of fully differential inputs with the convenience of a two wire hookup.

Although differential inputs are often preferable to single ended inputs, there are occasions when the floating nature of a differential input can confound attempts to make a reading. In those cases, the CIO-DAS48-PGA inputs can be converted to modified differential.

Examine the CIO-DAS48-PGA board. Near the 50 pin connector are positions for optional Single Inline Packages (SIP) of 10K resistors. Installing the SIP in RN7, RN8 and RN9 converts the analog inputs from fully differential to modified differential with a 10K reference to ground.

ALL THREE SIPS MUST BE INSTALLED. IT IS NOT POSSIBLE TO MIX CHANNELS.

Once the SIPs are installed, signal connections require on Signal Source Hi be connected to Channel N HI and signal source low be connected to Channel N LOW. No connection to LLGND need be made.

NOTE: *Special instructions and solder are packaged with the 10K SIP. Follow the installation instructions carefully and use the solder provided. Use of other solder, or failure to follow instructions will probably result in a degradation of the analog input's accuracy and will require out-of-warranty repair.*

5.5 CURRENT LOOP MEASUREMENTS

Before current loop measurements are made, the resistor SIP kit, CIO-DAS48-ISIP must be purchased and installed. Once installed, the inputs of the CIO-DAS48-PGA are committed to current measurement and may no longer be used for voltage measurement.

The SIPs RN7, RN8 and RN9 must NOT be installed if the board is to be used for current measurement. Or, if previously installed, must be removed.

Removal of the ISIPs restores the CIO-DAS48-PGA inputs to voltage measurement. Removal must be done by clipping off the SIPs. If you want to de-solder the SIPs the board must be returned to the factory.

It is not possible to install only a portion of the ISIPs and have a mixture of current and voltage inputs. You must install all 6 SIPs from the CIO-DAS48-ISIP package and set the MODE V-I jumper to I. ISIPs are installed in RN1, RN2, RN3, RN4, RN5, and RN6.

NOTE: *Special instructions and solder are packaged with the CIO-DAS48-ISIP kit. Follow the installation instructions carefully and use the solder provided. Use of other solder, or failure to follow instructions will probably result in a degradation of the analog input's.*

NOTE: The selection of the ISIPs is critical. Variations in either value or tolerance from those supplied in the CIO-DAS48-ISIP will result in measurement inaccuracy in relation to the operation of the CIO-DAS48-PGA current measurements as described here.

6 PROGRAMMING

Programming the CIO-DAS48-PGA is simple because the CIO-DAS48-PGA is capable of only 3 functions. All three are accessable through I/O reads and writes of the four I/O registers. Th three function are:

- Set programmable gain amp.
- Set a channel.
- Trigger 12 bit or 8 bit conversion.
- Read A/D data which is valid when EOC is true.

There are programming examples on the disk supplied with the board. The examples may be run and may be incorporated into your programs as subroutines.

The details of the I/O registers and functions are in the next section.

EXAMPLE SUBROUTINES IN BASIC

```
BASE% = &H300                          'Set base address to 300 Hex.

GAINSET:
    OUT(BASE% + 3) GAIN%               'Send gain code to gain register.
    RETURN

CHANSET:
    OUT(BASE% + 2), CHAN%              'Set channel to CHAN%.
    RETURN


ACQUIRE:
    OUT (BASE% + 1), 0                 'Trigger a conversion
      DO:
      LOOP WHILE INP(BASE% + 2) > 127  'Check EOC bit.
    XL% = INP(BASE%)                   'Get LSB
    XH% = INP(BASE% + 1)               'Get MSB
    CODE% = (XH% * 16 + XL% / 16)      'Convert to a value 0 to 4095
    RETURN
```

7 CIO-DAS48-PGA CONTROL & DATA REGISTERS

The CIO-DAS48-PGA is controlled and monitored by writing to and reading from 4 consecutive 8 bit I/O addresses. The first address, or BASE ADDRESS, is determined by setting a bank of switches on the board.

The register descriptions follow the format:

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	CH8	CH4	CH2	CH1

Where the numbers along the top row are the bit positions within the 8 bit byte and the numbers and symbols in the bottom row are the functions associated with that bit.

To write to or read from a register in decimal or HEX, the following weights apply:

BIT POSITION	DECIMAL VALUE	HEX VALUE
0	1	1
1	2	2
2	4	4
3	8	8
4	16	10
5	32	20
6	64	40
7	128	80

To write control words or data to a register, the individual bits must be set to 0 or 1 then combined to form a Byte. Data read from registers must be analyzed to determine which bits are on or off.

The method of programming required to set/read bits from bytes is beyond the scope of this manual. It will be covered in most Introduction To Programming books, available from a bookstore.

In summary form, the registers and their function are listed on the following table. Within each register are 8 bits which may constitute a byte of data or 8 individual bit set/read functions.

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 - 12(LSB)	Start 8 bit A/D conversion
BASE + 1	A/D Bits 1(MSB) - 8	Start 12 bit A/D conversion
BASE + 2	EOC, MUX Address	MUX address
BASE + 3	Gain Status, SINGLE/DIFF Switch	Programmable gain control

7.1 A/D DATA & START CONVERSION REGISTERS

BASE ADDRESS Example, 300 HEX, 768 Decimal

7	6	5	4	3	2	1	0
A/D9	A/D10	A/D11	A/D12 LSB	0	0	0	0

A read/write register.

READ

On read, it contains the least significant 4 digits of the Analog input data.

These 4 bits of analog input data must be combined with the 8 bits of analog input data in BASE + 1, forming a complete 12 bit number. The data is in the format 0 = minus full scale. 4095 = +FS.

WRITE

Writing any data to the register causes an immediate 8 bit A/D conversion.

BASE ADDRESS + 1 301 HEX, 769 Decimal

7	6	5	4	3	2	1	0
A/D1 MSB	A/D2	A/D3	A/D4	A/D5	A/D6	A/D7	A/D8

READ

On read the most significant A/D byte is read.

The A/D Bits code corresponds to the voltage on the input according to the table below.

DECIMAL	HEX	BIPOLAR	UNIPOLAR
4095	FFF	+ Full Scale	+ Full Scale
2048	800	0 Volts	1/2 Full Scale
0	0	- Full scale	0 Volts

WRITE

Writing to this register starts a 12 bit A/D conversion.

A note of caution: Place several NO-OP instructions between consecutive 12 bit A/D conversions to avoid over-running the A/D converter.

7.2 STATUS AND CONTROL REGISTER

BASE ADDRESS + 2 302 HEX, 770 Decimal

This register address is two registers, one is read active and one is write active.

READ = STATUS

7	6	5	4	3	2	1	0
EOC	0	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

EOC = 1 the A/D is busy converting and data should not be read.

EOC = 0 the A/D is not busy and data may be read.

MUX 5 to MUX 0 is the current multiplexor channel. The current channel is a binary coded number between 0 and 47 for single ended inputs or between 0 and 23 for differential inputs.

WRITE = CONTROL

7	6	5	4	3	2	1	0
0	0	MUX5	MUX4	MUX3	MUX2	MUX1	MUX0

MUX5 to MUX0. Set the current channel address by writing a binary coded number between 0 and 47 to these five bits.

NOTE: Every write to this register sets the current A/D channel MUX setting to the number in bits 5-0.

7.3 PROGRAMMABLE GAIN REGISTER

BASE ADDRESS + 3 303 HEX, 771 Decimal

The addition of a software programmable register which controls the input amplifier allows you to select unipolar/bipolar ranges and gains of 1, 2, 4 or 8 via software command.

The register's layout when written to is :

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
X	X	X	X	R3	R2	R1	R0

The register's layout when read from is :

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
MUXM	0	0	0	R3	R2	R1	R0

MUXM = Mux Mode. This bit = 0 when the channel configuration switch is set for 24 differential channels. It is = 1 when the switch is set for 48 single ended channels. This is a read-back only bit and has no ability to control the channel configuration.

R3-R1 = The programmable Gain/Range setting. The gain/range of the board is controlled by writing a control code to the register. The codes are:

These are the ranges available for the CIO-DAS48-PGA. Gains of 0.5, 1, 2, 4 & 8 are often called binary gains.

UNI-POLAR			CONTROL CODES					
Gain	Rang i	Range V	Dec	Hex	R3	R2	R1	R0
1	4-20 mA	0-10	1	1	0	0	0	1
2	2-10 mA	0-5	3	3	0	0	1	1
4	1-5 mA	0-2.5	5	5	0	1	0	1
8	.5-2.5mA	0-1.25	7	7	0	1	1	1

While the current input ranges are available in unipolar mode, they are not available in bipolar mode

BI-POLAR		CONTROL CODES					
Gain	Range V	Dec	Hex	R3	R2	R1	R0
0.5	±10	8	8	1	0	0	0
1	±5	0	0	0	0	0	0
2	±2.5	2	2	0	0	1	0
4	±1.25	4	4	0	4	0	0
8	±0.625	6	6	0	1	1	0

To set the input range of the CIO-DAS48-PGA board, select the desired range from the table and write the code in decimal or hexadecimal to base address + 3. Here is an example in BASIC.

```
100 OUT &H303, 2                    'Set gain = ±2.5V range.
```

8 SPECIFICATIONS

8.1 POWER CONSUMPTION

+5V Supply	150 mA typical / 200 mA max.
+12V Supply	None
-12V Supply	None

8.2 ANALOG INPUTS

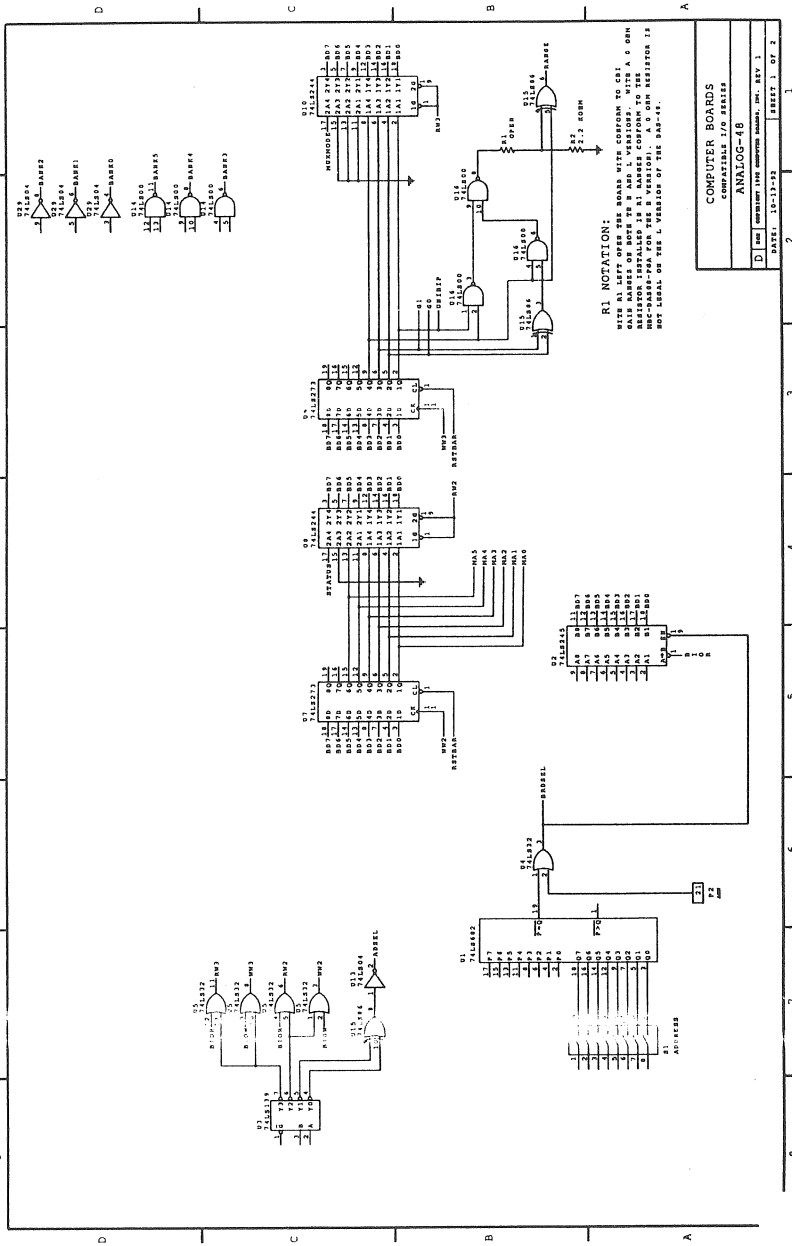
# Channels	48 Single Ended, or, 24, Differential or modified differential. Selected by installation or lack of SIP resistors which tie channel Lo to GND through a 10K resistor.
Resolution	12 bits, 4095 divisions of full scale.
Accuracy	0.01% of reading +/- 1 bit.
Type	Successive approximation
Speed	25 uSec - AD574
Monotonicity	Guaranteed over operating temp.
Linearity	+/- 1 bit
Ranges	Programmable - See charts
Overvolatge	+/- 30 Volts Continuous
Input Current	100 nA max @ 25 deg. C.
Input Impedence	10 Meg Ohms
Gain Temp. Coef.	+FS +/- 25 ppm/deg C -FS +/- 10 uV/deg C
Zero Drift	10 ppm/deg C max.
Gain Drift	50 ppm/deg C max.

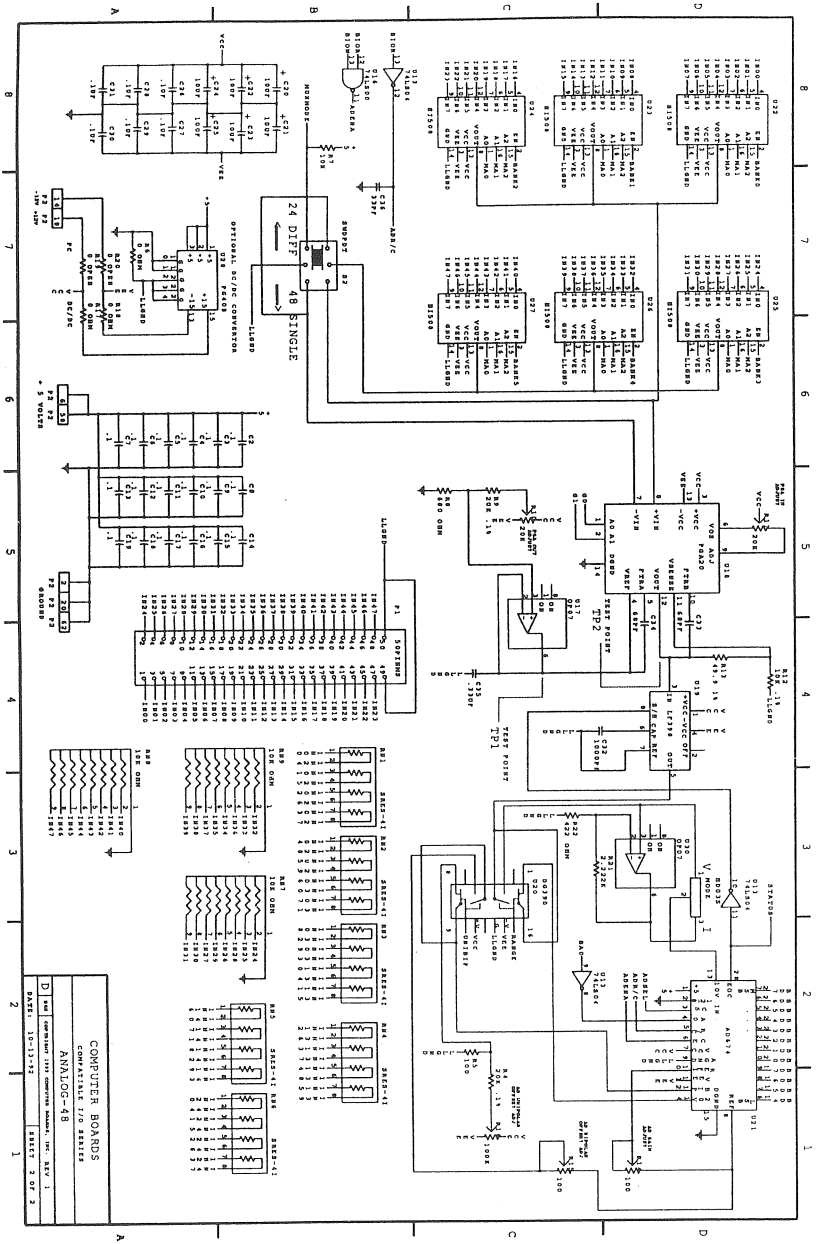
8.3 SAMPLE & HOLD AMP.

Acquisition Time	15 uSec to 0.01%
Dynamic error	1 bit @ 2000 V/Sec

8.4 ENVIRONMENTAL

Operating Temperature	0 - 50 deg C
Storage Temperature	-20 to 70 deg C
Humidity	0 to 90% non-condensing
Weight	5 oz


COMPUTER BOARDS
COMPATIBLE I/O SERIES
ANALOG-48
R1 NOTATION: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COMPATIBLE I/O SERIES
ANALOG-48
DATE: 12-13-95
SHEET 2 OF 2

10 ANALOG ELECTRONICS

This short, simple introduction to the analog electronics most often needed by data acquisition board users covers a few key concepts. They are:

- Voltage dividers.
- Differential vs. Single Ended Inputs.
- Isolation vs. Common Mode Range
- Low pass filters for analog and digital inputs.
- A/D Resolution
- Conversion to Engineering units.
- Noise; sources and solutions.

Each deals with the impact on measurements made with data acquisition boards. If you are truly interested in the subject of data converters and analog electronics, Radio Shack has written an excellent Op Amp handbook and has an Op Amp experimenters kit.

A more advanced treatment may be found in the Analog-Digital Conversion Handbook (32.95) and the Transducer Interfacing Handbook ($14.50) published by Prentice-Hall.

10.1 VOLTAGE DIVIDERS

If you wish to measure a signal which varies over a range greater than the input range of an analog or digital input, a voltage divider can drop the voltage of the input signal to the level the analog or digital input can measure.

A voltage divider takes advantage of Ohm's law, which states,

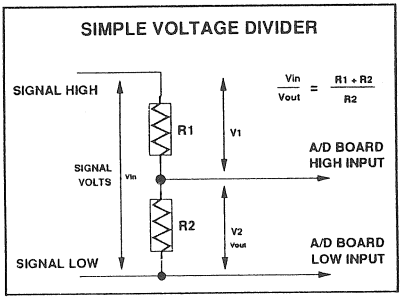
Voltage = Current * Resistance

and Kirkoff's voltage law which states,

The sum of the voltage drops around a circuit will be equal to the voltage drop for the entire circuit.

Implied in the above is that any variation in the voltage drop for the circuit as a whole will have a *proportional* variation in all the voltage drops in the circuit.

A voltage divider takes advantage of the fact that the voltage across one of the resistors in a circuit is proportional to the voltage across the total resistance in the circuit.
The trick to using a voltage divider is to choose two resistors with the proper proportions relative to the full scale of the analog or digital input and the maximum signal voltage.



The phenomena of dropping the voltage proportionally is often called attenuation. The formula for attenuation is:

Attenuation =	R1 + R2 -------- R2	The variable *Attenuation* is the proportional difference between the signal voltage max and the full scale of the analog input.
2 =	10K + 10K ---------- 10K	For example, if the signal varies between 0 and 20 volts and you wish to measure that with an analog input with a full scale range of 0 to 10 volts, the *Attenuation* is 2:1 or just 2.
R1 =	(A - 1) * R2	For a given attenuation, pick a handy resistor and call it R2, then use this formula to calculate R1.

Digital inputs also make use of voltage dividers, for example, if you wish to measure a digital signal that is at 0 volts when off and 24 volts when on, you cannot connect that directly to the CIO-AD digital inputs. The voltage must be dropped to 5 volts max when on. The *Attenuation* is 24:5 or 4.8. Use the equation above to find an appropriate R1 if R2 is 1K. Remember that a TTL input is 'on' when the input voltage is greater than 2.5 volts.

IMPORTANT NOTE: The resistors, R1 and R2, are going to dissipate all the power in the divider circuit according to the equation Current = Voltage / Resistance. The higher the value of the resistance (R1 + R2) the less power dissipated by the divider circuit. Here is a simple rule:

For Attenuation of 5:1 or less, no resistor should be less than 10K.

For Attenuation of greater than 5:1, no resistor should be less than 1K.

The CIO-TERMINAL has the circuitry on board to create custom voltage dividers. The CIO-TERMINAL is a 16" by 4" screw terminal board with two 37 pin D type connectors and 56 screw terminals (12 - 22 AWG). Designed for table top, wall or rack mounting, the board provides prototype, divider circuit, filter circuit and pull-up resistor positions which you may complete with the proper value components for your application.

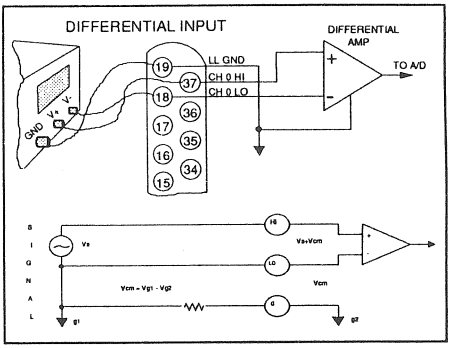
10.2 DIFFERENTIAL & SINGLE ENDED INPUTS

Two type of analog inputs are commonly found on A/D boards, they are differential and single ended. Single ended is the less expensive of the two.

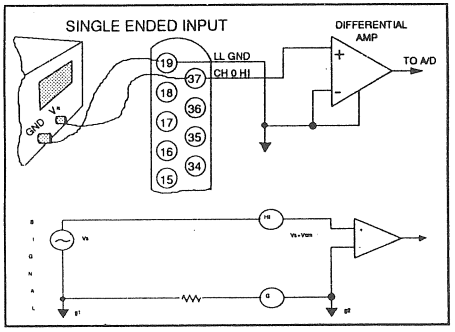
COMMON MODE RANGE

Differential inputs have a common mode range (CMR) (Vcm). Single ended inputs have no CMR . Common mode range is the voltage range over which differences in the low side of the signal and A/D input ground have no impact on the A/D's measurement of the signal voltage. A differential input can reject differences between signal ground and PC ground.

Shown here is a CIO-AD16 in differential mode.



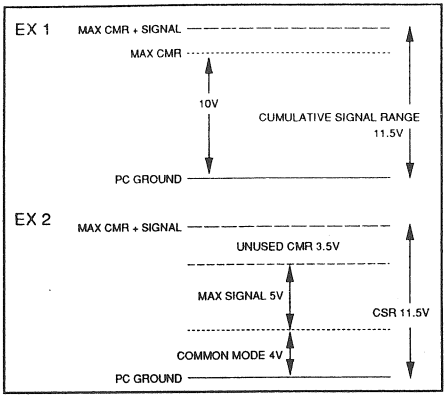
A single ended input has no common mode range because there is only one LOW wire, which is assumed to be at the same level at the signal and at the A/D board.



The maximum difference which may be rejected is the CMR.

For example, the CIO-AD16 has a common mode plus signal range of 11.5 volts, common mode not to exceed 10 volts.

This specification is illustrated graphically here and will be referred to as **Cumulative Signal Range (CSR)**.



Most manufactures of A/D boards specify the CMR directly from the component data sheet, ignoring the effect of the board level system on that specification. A data sheet of that type might claim 10 volts of CMR. Although this is a factual specification and the designer of the board (or other EE) would be able to translate that into a systems specification, most A/D board owners are confused or mislead by such specs.

COMMON MISUNDERSTANDINGS

The CMR specification of a differential input is often confused with an isolation specification, which it is not. It makes sense. doesn't it, that 10 volts of CMR is the same as 10 volts of isolation? No. The graph above shows why.

Also, failure to specify the common mode plus signal *system* specification leads people to believe that a DC offset equal to the component CMR can be rejected regardless of the input signal voltage. It cannot as the graph above illustrates.

When is a differential input useful? The best answer is whenever electromagnetic interference (EMI) or radio frequency interference (RFI) may be present in the path of the signal wires. EMI and RFI can induce voltages on *both* signal wires and the effect on single ended inputs is generally a voltage fluctuation between signal high and signal ground.

A differential input is not affected in that way. When the signal high and signal low of a differential input have EMI or RFI voltage induced on them, that ***common mode voltage*** is rejected, subject to the system constraint that common mode plus signal not exceed the A/D board's CSR specification.

GROUND LOOPS

Ground loops are circuits (E=I*R) created when the signal ground and the PC ground are not the same. Ground loop inducing voltage differential may be a few volts of hundreds of volts. They may be constant or transient (spikes). A differential input will prevent a ground loop as long as the CSR specifications is not exceeded.

If ground differences greater than the CMR are encountered, isolation is required.

WHY USE SINGLE ENDED?

Unanswered still is the question of why use single ended inputs? First, single ended inputs require fewer parts so they cost less money. On an A/D board the parts cost to go from 16 single ended channels to 16 differential channels is about $6.00 so that cannot be the reason. The real reason is connector space. Single ended inputs require one analog high input per channel and one LLGND shared by all inputs. Differential inputs require signal high and signal low inputs for each channel and one common shared LLGND.

Single ended inputs save connector space, parts cost and in all cases where there is no common mode or EMI/RFI they work just as well as differential inputs and are less complex to wire up.

10.3 LOW PASS FILTERS

A low pass filter is placed on the signal wires between a signal and an A/D board. It stops frequencies greater than the cut off frequency from entering the A/D board's analog *or* digital inputs.

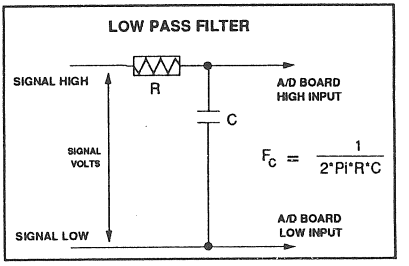
The key term in a low pass filter circuit is **cut off frequency**. The cut of frequency is that frequency above which no variation of voltage with respect to time may enter the circuit. For example, if a low pass filter had a cut off frequency of 30 Hz, the kind of interference associated with line voltage (60Hz) would be filtered out but a signal of 25Hz would be allowed to pass.

Also, in a digital circuit, a low pass filter might be used to de-bounce an input from a momentary contact button pushed by a person.

A low pass filter may be constructed from one resistor (R) and one capacitor (C). The cut off frequency is determined according to the formula:

$$F_c = \frac{1}{2 * Pi * R * C}$$

$$R = \frac{1}{2 * Pi * C * F_c}$$



10.4 A/D RESOLUTION & ENGINEERING UNITS

Resolution is specified in bits, such as 8, 10 or 12 bits. The 12 bits are really a power of 2 indicating the number of divisions of full scale the converter can resolve. For example, a 12 bit converter can resolve (2^12 - 1) = 4095 divisions of full scale. If the input of the board were +/- 5 volts full scale, each of the 4095 steps would be equal to 0.00244 volts.

Reading from the A/D converter would be thus:

Converter #	Volts
4095	5.0
4094	4.9976
4093	4.9951
2028	0.0
1	- 4.9976
0	- 5.0

The concept of resolution is the ability to differentiate between one voltage and another. Obviously, the more bits of resolution (13 bits = 8192 counts) the more divisions of full scale. The more divisions of full scale the finer the measurement.

ENGINEERING UNITS

When a program uses an A/D board to acquire data, the data file is filled with numbers like those above.

To translate the A/D numbers back into the engineering units of the original measurement, we need to know:

The sensor's voltage output per engineering unit.

The full scale range of the board at the time the measurement was made.

The resolution of the converter.

Here is an example from the application note on interfacing a Voland TA to a PC found elsewhere in this manual.

The TA measures resistance in grams between +500 and -500 grams.

The voltage output of the instruments is +2.5 volts to -2.5 volts.

The voltage output corresponds to the grams of pressure exactly, so:

+/- 500 grams = 1000 grams.

+/- 2.5 volts = 5 volts.

5 volts / 1000 grams = 0.005 volts per gram.

The A/D was set for +/- 2.5 volts = 5 volts full scale.

5 volts / 4095 counts = 0.00122 volts per bit.

If the number in the file for one reading was 3061, then

3061 * 0.00122 = 3.7632 volts.

3.7632 volts / 0.005 volts per gram = 735 grams.

Now shift from full scale to +/- scale.

735 grams full scale - 500 = 235 grams of positive pressure.

It may look like a lot of steps because it is presented that way here for clarity only. It could be expressed as a single equation in a spreadsheet.

10.5 NOISE

Noise is unavoidable in PC based data acquisition systems. There is board induced noise which can be measured by shorting an analog input to ground and taking a series of readings and plotting them in a histogram. There is EMI and RFI induced noise along the path of the signal wires. There is also noise at the signal source itself. All these sources of noise combine to create a region of uncertainty around the signal value.

Our objective here is to discover the sources of noise and discuss the means to reduce it.

SOURCES OF NOISE

The first source of noise is the board itself. Manufacturers of A/D boards quote component specifications in their data sheets but rarely quote a system specification for general accuracy and noise. The reasons the system is not specified are that the system specification would be less accurate than component specification and that system specifications must also specify the conditions under which the specification was made. That means the PC, the PC's power supply and the connection to the front end.

No one likes to admit it but it is true. Take some very good components, put them on a circuit board and place that board in a PC and the system will be less accurate than the individual components. I have seen 12 bit A/D boards with the same components as a DAS-16 with as little as 9 bits of accuracy, due to board noise.

The system specification for the CIO-AD16 and CIO-DAS48-PGA is plus or minus 1 LSB. That means that if an analog input is tied to ground and the CIO-AD16 is on a bipolar scale, the reading will be 2048 90% of the time. The other 10% of the readings will be 2047 and 2049, which is +/- count (LSB). This is actually not very different from the component specifications.

You can verify this by grounding an analog input channel to LLGND and taking 1000 readings then plotting a histogram of those readings.

If your histogram is not +/- 1 LSB, check the +/- 12V PC power supply voltages or call Computer Boards' Tech Support.

SIGNAL WIRE NOISE

Signal wires, especially single ended inputs, are subject to EMI and RFI, both of which can induce noise on the wires carrying the transducer signal to the CIO-AD board. Fortunately, signal wire noise is often localized and can be reduced by repositioning the signal wire run.

To check for signal wire noise, first, short analog channel 0 to low level ground[1] at the connector and take 10,000 samples and plot the histogram. This is the best the signal can be and is what you will try to achieve with the signal wires in place.

After you have an ideal case histogram, remove the short between analog input 0 and low level ground. Attach the signal wires to the CIO-AD board inputs and run them to the sensor. Do not connect the sensor yet, just short the analog input(s) to LLGND.

Take data for the histogram and compare it to the best case data taken previously. If it shows noise, you can try to eliminate the noise by doing the following:

- Move the signal wires, trying to locate a 'quiet' run.
- Use a shielded twisted pair as the signal wire. Attach the shield at the PC **only.** If the shield is attached at both the PC and the sensor it may create a ground loop and add to signal interference.

SENSOR NOISE

When the signal wires have been tested and characterized for signal quality, connect the sensor and provide a known level to the sensor (ice bath for temp., etc.) then take data for the histogram plot. If additional noise has been introduced by the sensor *which exceeds the sensor specifications*, you can try moving the sensor or electrically isolating it from the device it is measuring.

SMOOTHING DATA

It is not always possible to eliminate all noise, especially with very low level sensors, but noise looks terrible when plotted and can raise doubts about otherwise excellent data.

There are two simple ways to eliminate noise from the data:

1) Apply a moving average to the data if you want to retain the same *apparent* accuracy.
2) Remove the information from the noisy range. For example, if the A/D is capable of , or, shift the data by the number of counts of noise. For example, if a 12 bit A/D converter is at +/- 5 volts (10 volts full scale) then one LSB = 10 / 4095 = 0.00244mV. If your system is inducing +/- 0.007mV of noise (+/- 3 counts), then just round all the readings by +/- 3 counts. In this way the reading's value reflects the true accuracy of the system.

11 PC ARCHITECTURE

The architecture of the PC will not have an impact on the speed or accuracy of A/D boards operating at or under 100KHz DMA and 12 bits of resolution; with a few small exceptions.

CPU SPEED

The only performance parameter affected by computer type are CPU speed dependent operations, such as the time to service an interrupt. These variations have nothing to do with the A/D board alone but because board, software and CPU form a system, the differences are noticeable. For example, a 4.77MHz PC/XT acquire data from one of our interrupt driven routines at about 4,000 samples per second maximum while a 20 MHz 386 PC will process the same software at 20,000 samples per second.

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1 Differential inputs must have CH Hi, CH Lo and LLGND shorted. Single ended inputs must have CH Hi shorted to LLGND.

PC/AT 16 BIT DATA BUS

The CIO-DAS48-PGA is fully compatible with both the XT's 8 bit data bus and the AT/386's 16 bit data bus.

TABLE OF I/O ADDRESS

HEX RANGE	FUNCTION	HEX RANGE	FUNCTION
000-00F	8237 DMA #1	2C0-2CF	EGA
020-021	8259 PIC #1	2D0-2DF	EGA
040-043	8253 TIMER	2E0-2E7	GPIB (AT)
060-063	8255 PPI (XT)	2E8-2EF	SERIAL PORT
060-064	8742 CONTROLLER (AT)	2F8-2FF	SERIAL PORT
070-071	CMOS RAM & NMI MASK (AT)	300-30F	PROTOTYPE CARD
080-08F	DMA PAGE REGISTERS	310-31F	PROTOTYPE CARD
0A0-0A1	8259 PIC #2 (AT)	320-32F	HARD DISK (XT)
0A0-0AF	NMI MASK (XT)	378-37F	PARALLEL PRINTER
0C0-0DF	8237 #2 (AT)	380-38F	SDLC
0F0-0FF	80287 NUMERIC CO-P (AT)	3A0-3AF	SDLC
1F0-1FF	HARD DISK (AT)	3B0-3BB	MDA
200-20F	GAME CONTROL	3BC-3BF	PARALLEL PRINTER
210-21F	EXPANSION UNIT (XT)	3C0-3CF	EGA
238-23B	BUS MOUSE	3D0-3DF	CGA
23C-23F	ALT BUS MOUSE	3E8-3EF	SERIAL PORT
270-27F	PARALLEL PRINTER	3F0-3F7	FLOPPY DISK
2B0-2BF	EGA	3F8-3FF	SERIAL PORT

12 DIAGNOSIS & DEBUG

Computer Boards maintains technical support lines staffed by experienced Electrical Engineers and Technicians. There is no charge to call and calls are returned promptly if you have called when the lines were busy.

Most of the problems encountered with data acquisition plug in boards can be solved over the phone.

Signal connection and programming are the common sources of difficulty and Computer Boards' Tech Support people can solve these type of problems with you, especially if you prepare for the call.

1) Have the phone near the PC where you can try the things we suggest.
2) Be prepared to open the PC, remove the board and read back or change switch and jumper settings.
3) Have a volt meter available to make measurements of the signals you are trying to measure and the signals on the board and PC power supply.
4) Isolate the program lines that are not working as you expect them to.
5) Have all the source code to the program you are having trouble with so preceding modes and prerequisite modes may be discussed.
6) Have the manual ready.
7) Have the software Utility diskette available so the revision # and programs can be checked.

THIS LITTLE BIT OF PREPARATION WILL SPEED DIAGNOSIS AND MAY SAVE YOU THE TROUBLE OF A CALL BACK.

If you would like to try a few things first, here is a list of common problems.

1) Check the voltage level of the signal between the signal high and signal low. It cannot exceed the full scale range of the board.
2) Check the voltage between the signal ground and the PC ground. It should be 0 volts.
3) Check other boards in your PC for address and interrupt conflicts.
4) Refer to the example programs for techniques and as a baseline to check code against.

PLEASE, NO RETURNS WITHOUT RMA NUMBERS

Please, and here is why.

It slows down the solution of your problem.

If we receive a return without an RMA number written on the outside of the box, the contents of the box will sit in receiving until a Tech Support person is able to reach you and determine the reason for the return.

We need to know what you want us to look for.

The RMA system is fully automated and all the Tech Support engineers have access to the information in it. They can track your RMA and discuss your return history with you. This is very valuable if the setup you are using is overloading inputs. We can spot that and discuss a solution.

13 HAYNES DIAGRAM

ADDRESS	READ FUNCTION	WRITE FUNCTION
BASE	A/D Bits 9 - 12(LSB)	Start 8 bit A/D conversion
BASE + 1	A/D Bits 1(MSB) - 8	Start 12 bit A/D conversion
BASE + 2	EOC, MUX Address	MUX address
BASE + 3	Gain Status, DIFF/SINGLE Switch	Programmable gain control