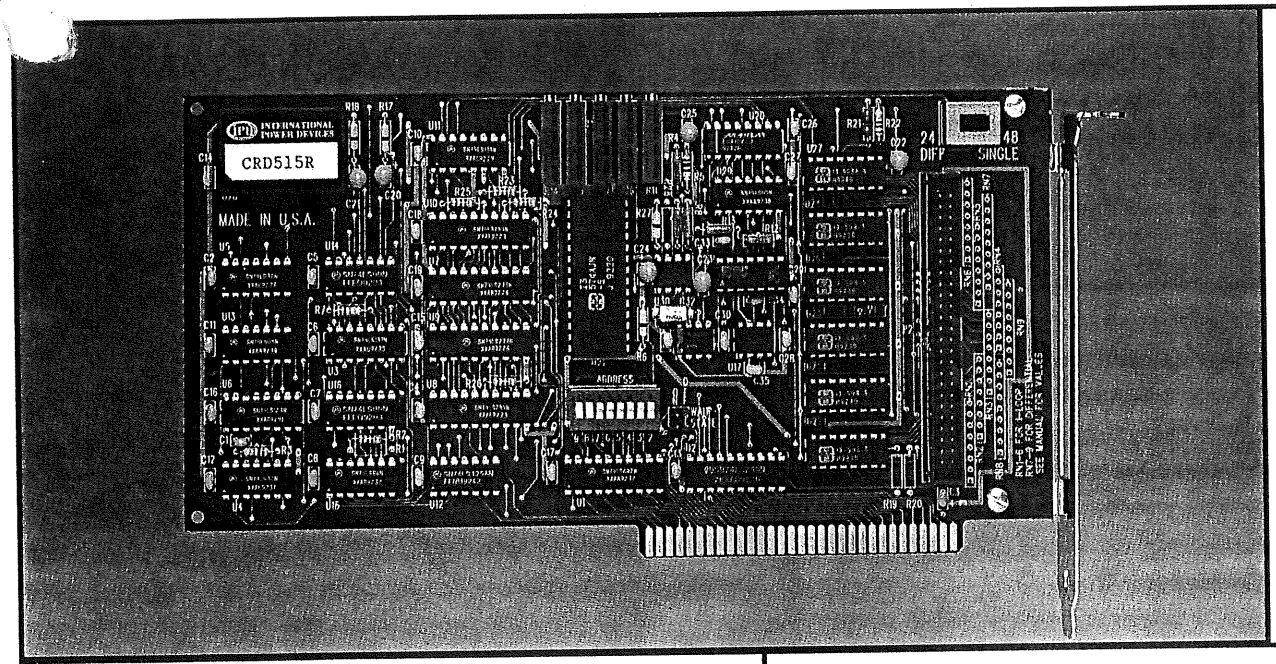
CIO-DAS48-PGA

48 Channel, 12 Bit Analog Input Board. Voltage Input with Programmable Gain or Full 12 Bit 4-20mA.



FULL 12 BIT RESOLUTION IN BOTH VOLTAGE *and* CURRENT RANGES

High Density, Voltage or Current

Designed for low speed, high density analog measurement, the CIO-DAS48 is especially suited for 4-20mA readings. The analog inputs may be configured as 48 single ended voltage, 24 differential voltage or 24 current sensing inputs. Installing resistor SIPs in the positions provided near the 50 pin header connector modify the input circuitry to work in one of the single ended, differential or current input modes.

Process control sensors with built in sending units often use 4-20mA current loop to communicate with the data acquisition system; a computer or programmable controller. Current loop transmission is noise immune. Electromechanical disturbances and RFI from AC voltage sources will not affect the signal level of a 4-20mA current loop. Noise immunity makes 4-20mA desirable in factory environments.

Most data acquisition boards are designed for voltage input only. They can easily be converted to current input with a shunt resistor but lose resolution in the process. For example, a 0-5V input may be converted to 0-20mA by placing a 250 Ohm precision resistor across the inputs (E/I=R, or, 5/0.02 = 250). If a 4-20mA loop is being monitored, 20% of the resolution is lost because the range 0-4mA is unused.

When installed, the current conversion SIPs provide full 12 bit resolution over the range 4-20mA.

The analog input circuit contains a programmable amplifier so the input range is under software control. Both voltage and current input ranges are programmable and although four current input ranges are available, it is likely that the 4-20mA range is the one you selected in.

I/O Connector and Cabling

A single 50 pin connector provides the interface to cables and screw terminal boards. The connector is a standard Amp 0.10" spacing header connector.

The inputs are arranged so that in differential mode channel high and channel low run side by side on the cable. In single ended mode each pin acts as an independent analog input. Pins 49 and 50 provide reference to low level ground, a requirement for both differential & single ended inputs.

A screw terminal, the CIO-MINI50, provides 12-20 AWG jaw-clamp type screw terminals on a 4"X4" board supplied with 1/2" standoffs. The CIO-MINI50 employs the same 50 pin male header as the CIO-DAS48.

Order cable C50FF-2 or custom lengths up to 10 feet to connect the CIO-DAS48 and CIO-MINI50 together.

Of course, you may eliminate the screw terminal board and direct wire signals to the CIO-DAS48 through a ribbon cable terminated with a 50 pin connector.

LLGND	50		49	LLGND
CH 47 HI / CH 23 LOW	48		47	CH HI 23
CH 46 HI / CH 22 LOW	46		45	CH HI 22
CH 45 HI / CH 21 LOW	44		43	CH HI 21
CH 44 HI / CH 20 LOW	42		41	CH HI 20
CH 43 HI / CH 19 LOW	40		39	CH HI 19
CH 42 HI / CH 18 LOW	38		37	CH HI 18
CH 41 HI / CH 17 LOW	36		35	CH HI 17
CH 40 HI / CH 16 LOW	34		33	CH HI 16
CH 39 HI / CH 15 LOW	32		31	CH HI 15
CH 38 HI / CH 14 LOW	30		29	CH HI 14
CH 37 HI / CH 13 LOW	28		27	CH HI 13
CH 36 HI / CH 12 LOW	26		25	CH HI 12
CH 35 HI / CH 11 LOW	24		23	CH HI 11
CH 34 HI / CH 10 LOW	22		21	CH HI 10
CH 33 HI / CH 9 LOW	20		19	CH HI 9
CH 32 HI / CH 8 LOW	18		17	CH HI 8
CH 31 HI / CH 7 LOW	16		15	CH HI 7
CH 30 HI / CH 6 LOW	14		13	CH HI 6
CH 29 HI / CH 5 LOW	12		11	CH HI 5
CH 28 HI / CH 4 LOW	10		9	CH HI 4
CH 27 HI / CH 3 LOW	8		7	CH HI 3
CH 26 HI / CH 2 LOW	6		5	CH HI 2
CH 25 HI / CH 1 LOW	4		3	CH HI 1
CH 24 HI / CH 0 LOW	2		1	CH HI 0

ANALOG INPUTS

The analog input section of the CIO-DAS48-PGA has been designed for flexibility and accuracy in a number of configurations and ranges. The analog signals are brought on board by a standard 50 pin header type connector directly to analog multiplexors. The multiplexors provides 48 channels of single ended input or 24 channels of differential input and are protected against 30 volts max.

A 2 uSec sample & hold captures the signal which is converted by a 574 A/D converter. The 12 bit A/D converter provides a resolution of 1/4095 parts of full scale.

The speed of data gathering is dependent on the CPU speed but in general may not exceed 20KHz on a fast 386 or 486 computer.

A/D conversions are initiated by a software trigger (write to Base + 1). The conversions may be paced by the personal computer system clock or the timer you have created under program control.

The CIO-DAS48-PGA is not designed for applications such as spectrum analysis or any signal analysis requiring precise sample intervals generated by an on-board pacer clock.

The CIO-DAS48-PGA is best utilized in process control or other applications where the A/D samples are initiated under program control.

Analog Input Ranges

The CIO-DAS48-PGA input range may be programmed as bipolar or unipolar in any of 5 ranges (0.5, 1, 2, 4 & 8). Given the A/D converter's standard +/-5V input range, this translates to input ranges of:

Gain	Bipolar	Unipolar	Unipolar Current
0.5	+/-10 V	N/A	N/A
1	+/-5 V	0 - 10 V	4-20 mA
2	+/-2.5 V	0 - 5 V	2-10 mA
4	+/-1.25 V	0 - 2.5 V	1-5 mA
8	+/-0.625 V	0 - 1.25 V	0.5-2.5 mA

SPECIFICATIONS

A/D Resolution	12 Bits
Channels	24 Differential (Voltage)
	48 Single Ended (Voltage)
	24 Current Input
Programmable Ranges	
Bipolar (Volts)	+/-10, +/-5, +/-2.5, +/-1.25, +/-0.625
Unipolar (Volts)	0-10, 0-5, 0-2.5, 0-1.25
Current (mA)	4-20, 2-10, 1-5, 0.5-2.5
Conversion Speed	25uS
Linearity	+/-1 Bit
Zero Drift	20 ppm /Deg C
Gain Drift	35 ppm /Deg C
Input Impedance	>100M ohm

I/O & Control Register Map

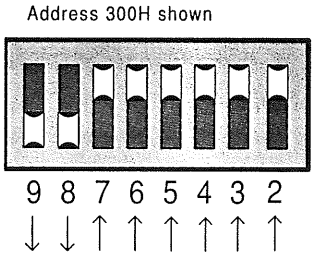
The I/O and control registers of the CIO-DAS48-PGA are very close to those of the CIO-DAS08-PGA. There are only two differences between the two board's registers. First, since the CIO-DAS48-PGA has 48 channels the MUX control register has three extra bits for a total of 6 (2^6=64). Second, the CIO-DAS48-PGA connector has no spare pins for counters or digital I/O and so has no control registers for digital I/O or counters. Because of the close compatibility, it is quite easy to adapt software to the CIO-DAS48-PGA.

The CIO-DAS48-PGA uses 4 I/O addresses:

Address	Read	Write
Base +0	A/D low byte	Start 8 Bit Conversion
Base +1	A/D high byte	Start 12 Bit Conversion
Base +2	Current Channel Selected	Set Channel Select Mux
Base +3	Gain & Range Setting	Set Gain & Range

Base Address

The I/O base address is set with a bank of switches contained in a single DIP switch. The switch selects the first address for the first registers on the board (A/D Low Byte/ Start Conversion).



Programming

The CIO-DAS48-PGA may be programmed directly with I/O write and read command providing control from BASIC, C and Pascal. It is quite easy to control the CIO-DAS48-PGA from any language that provides I/O instructions because of the simple register structure.

For those who prefer a language driver or library, the CIO-DAS48 is supported by the Universal Driver programming language support package (please see the data sheet).

Following is an example of register programming a single 12 bit A/D from a Basic subroutine:

```
ACQUIRE:
    BA% = &H300                          'Set Base to 300 Hex
    OUT (BA% +1), 0                      'Initiate a 12 bit A/D
    LOOP WHILE INP(BA% + 2 > 127)        'Wait for End of Conversion
    LSB% = INP(BA% + 0)                  'Read the LS Byte
    MSB% = INP(BA% + 1)                  'Read the MS Byte
    AD% = MSB% * 16 + LSB% / 16          'Combine to 12 bit value
    RETURN
```

Ordering Guide

48 Channel A/D board, gain of 0.5,1,2,4,8	CIO-DAS48-PGA
50 Connector Screw Terminal Board	CIO-MINI50
50 Conductor Cable, 2 ft. length	C50FF-2
50 Conductor Cable, Custom Length	C50FF-##